Investigation into Digital Circuit Design with $GaAs/Ga_2O_3$ Heterostructure MOSFETs

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Abstract

In this thesis, GaAs heterostructure MOSFETs are investigated as a potential technology for digital circuit design. The devices under investigation are 0.6 μm gate length, enhancement mode, heterostructure MOSFETs, with a high-κ dielectric (Ga_2O_3), and an InGaAs channel. Historically silicon CMOS technology has been the natural choice for digital circuits, however the realisation of GaAs MOSFET digital circuits could allow full integration of RF, optoelectronic and digital circuits on a single system-on-chip. Additionally, there are potential performance advantages in using GaAs due to it's high electron mobility. For the first time compact models of complimentary GaAs/Ga_2O_3 MOS are developed to enable an investigation into establishing a digital design methodology for GaAs MOS.

Drift-diffusion models are developed and calibrated to measured device data. These models then provide information on the necessary device parameters to build compact models of these devices. BSIM3v3.2 compact models are developed based on this to enable GaAs MOS technology to be investigated using standard circuit design tools. The compact models have been adapted to ensure that they are physically relevant for GaAs devices. This includes some necessary approximations using effective medium theory. Further adjustments, or ratio corrections, are introduced to ensure that the internal physical parameters of BSIM will be correct.

The models are compared to similarly-sized silicon devices to investigate the difference in performance between GaAs and silicon MOSFETs. As expected, the GaAs NMOS devices demonstrate improvements in drive current over silicon. However, the GaAs PMOS devices do not offer this advantage due to low hole mobility. Therefore, as a consequence of the high mobility ratio in GaAs, it is important to consider alternative digital design methodologies to CMOS to optimise performance.

The performance of benchmark circuits is investigated for this technology in

various digital design styles including CMOS, NMOS saturated enhancement load, and NMOS precharge. GaAs digital circuits gain a significant advantage in using alternative design styles to CMOS due to the relatively poor performance of the PMOS devices. In using the alternative styles the number of PMOS devices used can be minimised, and it is shown that NMOS precharge offers both speed and power advantages for this technology.

The particular GaAs technology investigated does not outperform silicon in terms of speed and power. However, it has allowed a methodology to be established for future device generations, where performance is anticipated to improve significantly.

For Jack

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Glossary

Acronyms

BSIM	Berkeley Short-Channel IGFET Model
C-V	Capacitance-Voltage
CMOS	Complementary Metal Oxide Semiconductor
DIBL	Drain Induced Barrier Lowering
DUT	Device Under Test
E/D	Enhancement-Depletion
E/E	Enhancement-Enhancement
FET	Field-Effect Transistor
FO	Fan-out
I-V	Current-Voltage
IC	Integrated Circuit
III-V	A group of materials which are compounds of elements in columns 13 and 15 (IUPC style) of the periodic table, e.g. GaAs
IP	Intellectual Property
IT	Information Technology
ITRS	International Technology Roadmap for Semiconductors

IUPAC	International Union of Pure and Applied Chemistry
MESFET	Metal Epitaxial Semiconductor Field Effect Transistor
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MOSHEMT	Metal Oxide Semiconductor High Electron Mobility Transistor
MOSHFET	Metal Oxide Semiconductor Heterostructure Field Effect Transistor
PHEMT	Pseudomorphic Hight Electron Mobility Transistor
SiP	System-in-Package
SoC	System-on-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
TEM	Transmission Electron Microscope
tphl	Time to Propagate a High to Low Signal
tplh	Time to Propagate a Low to High Signal

Constants

ϵ_0	Permittivity Constant, 8.85×10^{-12} F/m [9]
$\kappa_{Ga_2O_3}$	Dielectric Constant of Ga_2O_3, 10 [4]
κ_{GaAs}	Dielectric Constant of GaAs, 13.1 [10]
κ_{SiO_2}	Dielectric Constant of SiO_2, 3.9 [7]
κ_{Si}	Dielectric Constant of Si, 11.7 [7]
k_B	Boltzman's Constant, $1.38 \times 10^{-23} J/K$ [9]
q	Elementary Unit of Charge, $1.6 \times 10^{-19} C$ [9]

Symbols

ϵ_{ox}	Permittivity of the Oxide
ϵ_s	Permittivity of the Semiconductor
κ	Dielectric Constant
κ_{eff}	Effective Dielectric Constant
κ_{ox}	Dielectric Constant of the Oxide
μ_n	Electron Mobility
μ_p	Hole Mobility
ϕ_m	Metal Work Function
ϕ_n	Quasi-Fermi Potential for Electrons
ϕ_p	Quasi-Fermi Potential for Holes
ϕ_s	Substrate Work Function
ψ	Electrostatic Potential
ψ_B	Fermi Potential in the Substrate
ρ_S	Charge Density
$\vec{J}_n$	Current Density of Electrons
$\vec{J}_p$	Current Density of Holes
C_{ox}	Oxide Capacitance
D_n	Diffusion Coefficient for Electrons
D_p	Diffusion Coefficient for Holes
L_{ds}	Distance between the gate and drain in a device.
L_{gs}	Distance between the gate and source in a device.

n	Electron Concentration
N_D^+	Ionised Impurity Density of Donors
N_A^-	Ionised Impurity Density of Acceptors
N_{ch}	Channel Doping Concentration
n_i	Intrinsic Carrier Concentration
N_s	Substrate Doping Concentration
p	Hole Concentration
Q_{dm}	Charge in Depletion Layer
T	Temperature
t_{ox}	Oxide Thickness
t_{ox}^{RC}	Oxide Thickness with Ratio Correction
U_n	Net Electron Recombination
U_p	Net Hole Recombination
V_{bs}	Bulk to source voltage
V_{ds}	Drain to source voltage
V_{fb}	Flat-band Voltage
V_{gs}	Gate to source voltage
V_{th}	Threshold Voltage
X_j	Width of Depletion Layer or Junction Depth
N_s^{RC}	Substrate Doping with Ratio Correction
Q_d	Drain Charge
Q_s	Source Charge

t_f	Fall Time
t_r	Rise Time
V_{dd}	Supply Voltage

Chemical Symbols

Al_2O_3	Aluminium Oxide
Ga	Gallium
Ga_2O_x	Gallium Oxide
GaAs	Gallium Arsenide
$Gd_3Ga_5O_{12}$	Gadolinium Gallium Arsenide
Ge	Germanium
H_2	Hydrogen
N_2	Nitrogen
O_2	Oxygen
Si_3N_4	Silicon Nitride
SiGe	Silicon Germanium
SiO_x	Silicon Oxide
TiWN	Titanium Tungsten Nitride

1 Introduction

1.1 Overview

The principle goal of this project was to investigate digital circuit design techniques for gallium arsenide (GaAs) heterostructure MOSFETs. This was achieved by developing physical and compact models of complimentary GaAs devices based on measured device data from Motorola (now Freescale). These models were then used to investigate the potential performance of GaAs digital circuits. This investigation was necessary due to the fundamentally different transport properties of GaAs devices compared to silicon, whose design methodologies are well understood.

GaAs/Ga_2O_3 MOSFET technology has been in development for many years, however so far the focus has been on device development via fabrication methods and theoretical modelling. There has been little work on circuit design methodologies for this technology to date.

This work first focuses on the methodology required to move from fabricated GaAs device results to circuit simulations. This then enables an investigation into appropriate digital design styles for this new technology paradigm. Hence, as future devices are developed, a method is in place for effective modelling, simulation, and circuit design with this technology. This is the first time that GaAs MOSFET devices have been taken this far through the design cycle. Therefore, this work

provides a first-look methodology for compact model development based on physical device modelling for GaAs MOSFETs, and for circuit design using these models.

1.2 Motivation

As silicon approaches its physical limit for device scaling, the industry is looking towards new structures and materials to provide continued advances in performance [11, 12]. In addition to striving towards smaller and faster digital circuits, increased system level integration is also a key objective.

The integration of RF, optoelectronic, and digital devices on to a single chip is a desirable goal. GaAs devices are currently used in both RF and optoelectronics applications, although historically silicon CMOS technology has dominated digital logic. The realisation of GaAs MOSFET digital circuits would allow the potential for a fully integrated system-on-chip platform. The challenges and benefits of this will be further discussed in sections 2.3.1 and 3.2.

There are also potential performance advantages in using GaAs and its tertiary compounds, due to the intrinsic transport properties of the materials. The electron mobility in GaAs for example is around six times greater than in silicon, however unconventional device structures are required to obtain the best performance, and the size of devices also effects optimum performance.

The ITRS roadmap now firmly places GaAs as a complementary technology to silicon for VLSI [11]. Therefore, it is crucial to develop methodologies for the design of GaAs MOS-based digital circuits, and to investigate how their operation might be optimised.

1.3 Thesis Outline

Chapter 2 introduces the business and management issues associated with this project and the semiconductor industry. The project motivation will be revisited in terms of industry goals, and the challenges associated with introducing new technologies to market will be discussed. Business and management topics such as effective team management, organisational structures, and redundancy, are discussed and illustrated with examples to relate these to the semiconductor industry.

This is followed, in chapter 3, by background information on the technical developments in this field along with a review of the key literature in the area.

The next three chapters describe the core technical work achieved in this project. In chapter 4, calibrated drift-diffusion models of GaAs MOSFETs are developed, based on fabricated device results by Motorola. The devices used for this investigation were 0.6 μm gate length, enhancement mode, heterostructure MOSFETs, with a high-κ dielectric (Ga_2O_3), and an InGaAs channel.

In chapter 5, compact models based on the data and the drift-diffusion results are developed. The models are created by adapting the industry standard BSIM3 silicon compact model to make it physically relevant for GaAs devices. The method and calculations for this are presented, along with discussion of the necessary assumptions that are made. Additionally, the concept of ratio correction is introduced to cope with inaccesable physical parameters in the BSIM model.

Using these compact models, circuit design with GaAs/Ga_2O_3 devices is then investigated in chapter 6. This includes a comparison of different circuit styles in both silicon and GaAs. The relative merits of the different styles are discussed and recommendations are made regarding GaAs digital design.

Finally, the key points and results will be concluded in chapter 7, along with a discussion of possible future work.

Rather than a separate theory chapter, any relevant theory has been distributed to the appropriate chapter. A list of acronyms, physical constants, symbols, and chemical symbols, is given in the glossary.

2 A Business & Management Perspective

2.1 Introduction

A key part of an EngD is to understand and assess the industry implications of the research work carried out. This involves having a knowledge of how the industry works and how it might respond to products and applications associated with research.

To help achieve this, time is spent working within both industry and academia. In addition, the inclusion of study towards one third (60 credits) of an MBA aids a more technical understanding of some of the relevant business areas. I chose to complete this by studying three modules at the Edinburgh Business School, Heriot Watt

University. The modules studied were Organisational Behaviour, Project Management, and Accounting.

I chose these modules to build my knowledge in areas that I have not had a chance to study before. Moreover, this combination of subjects complemented each other in view of looking towards my career development plan of eventually managing technical teams. Figure 2.1 summarises the key points and how these fit together.

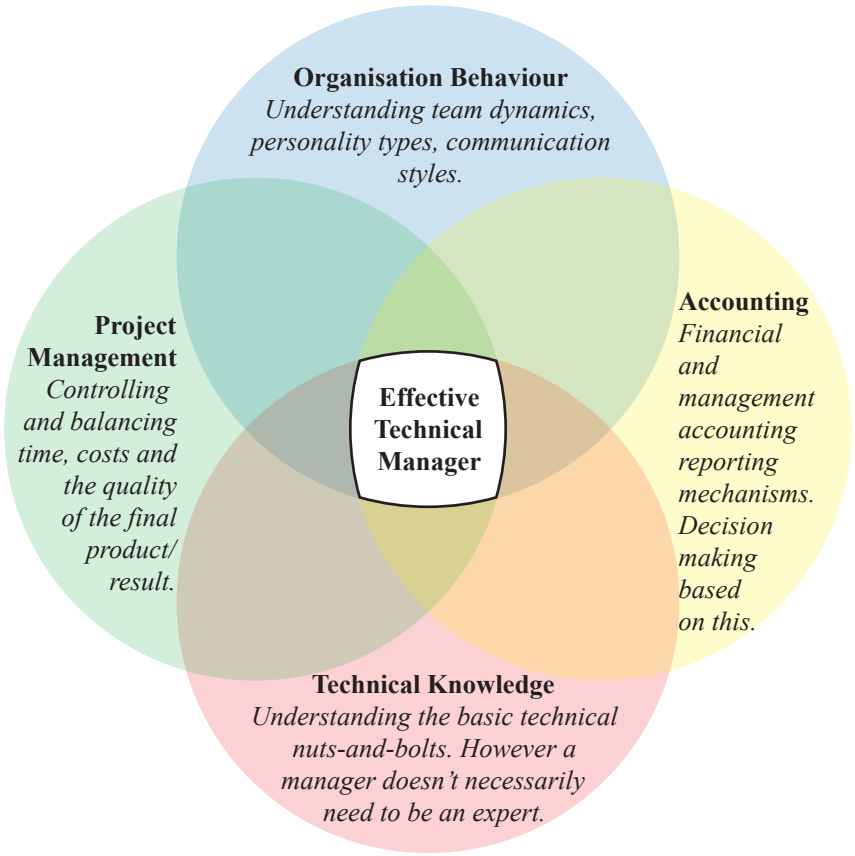


Figure 2.1: Components of effective technical team management.

Organisational Behaviour offers an insight on different personality types and communication styles, and how to select a team with and effective working dynamic. If a team is to be balanced, work well together, and have a good network of support then these skills are critical. The significance of this will be discussed further in section 2.5. Project management emphasises the importance of balancing time, cost, and quality when working towards the goals of a team. These skills are particularly

pertinent to managing project teams, however they are also generally applicable to team management. Aspects of this will be discussed in section 2.6. In accounting, along with a strong grounding in the fundamentals of financial accounting, the importance of management accounting reporting techniques was emphasised, and the use of these reports by managers and team leaders in decision making.

In this chapter I shall first discuss the necessary redirection of my research project, including the work that I completed when based with Motorola along with the circumstances surrounding the necessary change in the direction of the project. The industrial context for this project and the key companies and institutions that are researching in this field will then be examined. Key areas in the MBA subjects studied, particularly those areas which I found relevant to my own EngD work, the electronics industry and academia will be discussed. Where possible, these will be illustrated with real examples from my own work experience. Finally, I shall detail some of the training and development events, and conferences that I have attended, as I consider this continuing professional development particularly pertinent in the context of completing the EngD.

2.2 Redirecting Research

This part of my research project was one of the most challenging. This EngD project started in a very different direction from that which is described in this thesis. In July 2003 once the MSc taught component of the EngD was completed I went to work at my sponsoring company, Motorola NCSG (Networking & Computing Systems Group). The EngD project was to be in the field of functional verification, involving topics such as code coverage analysis, software programming and algorithm design.

The motivation for the verification project was that due to the increasing complexity of hardware designs, it is not uncommon for functional verification to take between 60-80% of the time and resources of a design project. With this large overhead on verification any reduction in the time and effort involved in this activity is of great benefit as it will save time, money and resources on a project. Code coverage figures are used as a metric to determine when functional verification is complete or has been done to an acceptable level. The two types of code coverage considered

were statement and expression coverage. Companies usually have guidelines as to what they consider acceptable percentages for these metrics, Motorola required all of its designs to have 100% statement coverage and 95% expression coverage. IP blocks in a design are individually tested, and then the design is tested as a whole. However the possibility of merging block level tests with system level tests reduces the amount of repeated work done in porting block tests to system level. There may be parts of the design that can only be tested at system level, but my belief was that re-using block level coverage results wherever possible would reduce the time involved in the hardware verification process. The primary software tool used for code coverage analysis at Motorola NCSG was a Cadence tool called *nccov*. I developed my own software to post-process the nccov results so that multi-level code coverage results could be merged. The software that I developed was used to compile results for a project that was running over the summer of 2003 at Motorola. Appendix A gives details of the resulting chip.

In September 2003 Motorola decided to spin-out part of its Semiconductor Products Services devision in to Freescale Semiconductor and make the remainder redundant. The Networking & Computing Systems Group was a part of this division and was made redundant. I shall discuss the reasons for, and effects of, such a restructuring process in section 2.7.

In October 2003 I began the GaAs MOSFET research project described in this thesis, still sponsored by Motorola but principally based at the University of Glasgow.

2.3 GaAs MOSFET Development

2.3.1 Industry Motivation for Research

When considering a new direction in research it is important to know who and where the target market for your technology is. This will depend greatly on the type of product being offered. For example, the market is somewhat different for a hardware IP block than for a packaged mobile phone. It is also important to consider whether the product is for a niche market or if it is more globally marketable. GaAs digital MOSFETs are currently a niche market, however their many benefits give them the

potential to have more widespread application in the future [13].

There are several reasons that make GaAs an appealing technology for digital design, as discussed in section 1.2. However, the most important from an industry standpoint is the potential integration of GaAs digital, optoelectronic and RF components on a single chip. Integration on a single chip generally means a reduction in the size of a system thus reducing packaging costs. Smaller and cheaper products are generally more desirable to consumers and manufacturers who would be the two potential markets for an integrated product of this nature. For example, GaAs HEMTs and MESFETs are currently used in mobile phones, PCs, and direct broadcast satellite receivers. Therefore, one example of an integrated GaAs SoC would be a mobile-on-a-chip.

The hard work in introducing such a new technology comes first and foremost in the development of the fabrication processes, and it will be shown in chapter 3 that this has been a long and difficult one. However, the technology is now coming to fruition, and will continue to improve as it matures.

The next thing to consider is how is will be integrated into existing design flows. It is important that this is achieved if the technology is to be used widely by digital designers. For example, by the time we have ascended the design hierarchy to digital IP designers working with hardware description languages, the change should be simply one of using a different technology file and cell library. Which is something designers already do when moving to a new silicon technology node. Therefore, the design tool flow at this level should see little change. For this to be successful, cell library components must be carefully designed to make the best use of the new technology. One of the goals in this project was to investigate how standard cell components might be optimally designed based on a physical understanding of such new technologies.

Finally, designers must be encouraged away from their silicon comfort zone. However, silicon design is facing new challenges in the nano-scale domain. Digital designers are now having to consider issues such as variability between devices, that were once only a problem for analogue designers. With these new problems perhaps people will be more open minded to alternative materials and design methodologies.

The main beneficiaries of such a new technology will not only be the foundries which offer the technology, but also fabless IP design companies. IP companies

who are able to provide new collections of IP blocks which take advantage of such a highly integrated platform will provide a quicker route to market for end-use designers wishing to prototype in the technology.

2.3.2 Key Companies and Institutes

Several companies and institutes made initial investigations into GaAs MOSFET technology. However many decided not to continue work in this area such as Fujitsu, the University of Newcastle upon Tyne, the National Cheng-Kung University and the IBM Thomas J. Watson Research Centre.

Much of the enabling chemistry based research for GaAs was done at AT&T Bell Laboratories (part of AT&T Bell Technologies) and the University of California San Diego. In 1996 AT&T Bell Technologies was spun-out as Lucent Technologies. In August 2000 Agere was incorporated as a subsidiary of Lucent Technologies and then spun-out in June 2002.

Much work in this field was also developed by Motorola, Inc. and then at Freescale Semiconductor when is was spun-out of the Semiconductor Products Services devision of Motorola.

Many of the key researchers in this field moved between the companies mentioned taking with them knowledge and collaborative partnerships. Currently Freescale (and, to some extent, Agere Systems, which is now part of LSI) is leading the development in GaAs devices for digital applications. Many of the key researchers who were a part of GaAs development at AT&T Bell Laboratories now work at Freescale and Agere.

Details of the major technical achievements related to the above will be presented in chapter 3.

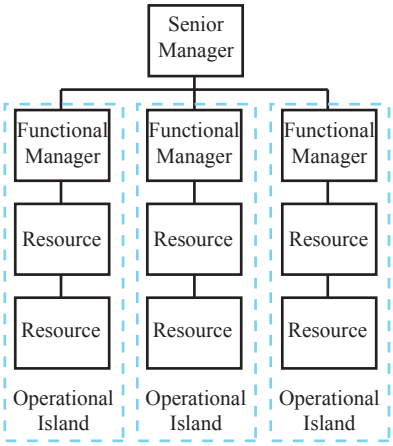
2.4 Management Structures

A key part of understanding how organisations function is understanding the different management structures they use. This is relevant in both industry and academia and was a key part in all of the business courses that I studied. There are three main structural models used; Functional, Project and Matrix (see figure 2.2). These models all have benefits and disadvantages and the type of structure that is most suitable will depend on the type of organisation.

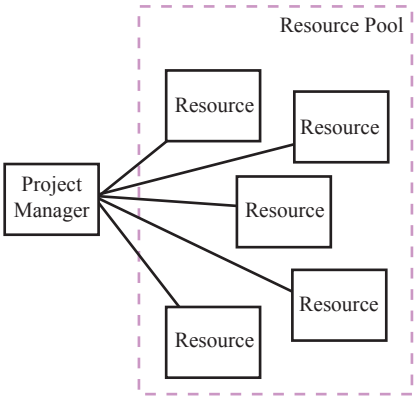
A purely functional structure is very common in large organisations (see figure 2.2(a)). It is a top down approach to management, with authority and accountability well defined. The level of authority is clearly defined by vertical position in the structure, the highest at the top, and individuals are accountable to those directly above them. This type of structure is preferred by organisations that have departments that perform either highly repetitive or highly specialised tasks. A solely functional structure is also preferred by organisations that require very clearly defined roles and responsibilities operating within a chain of command, such as government institutions. It is, however, too inflexible for many institutions where some degree of cross functional collaboration is necessary. Operational islands can be a problem in this type of structure as there is little or no communication and collaboration between functional divisions as all communication goes directly up and down the management structure.

A project structure is quite the opposite to a functional structure (see figure 2.2(b)), as projects by their nature are finite and usually cross-functional. A project manager usually has a pool of resources to call on for the project's duration and it is their responsibility to utilise these resources in such a way that the project is completed on time. A pure project structure is extremely flexible and responsive to change. Communication between management and staff and the reporting mechanisms are also much simpler in a project structure.

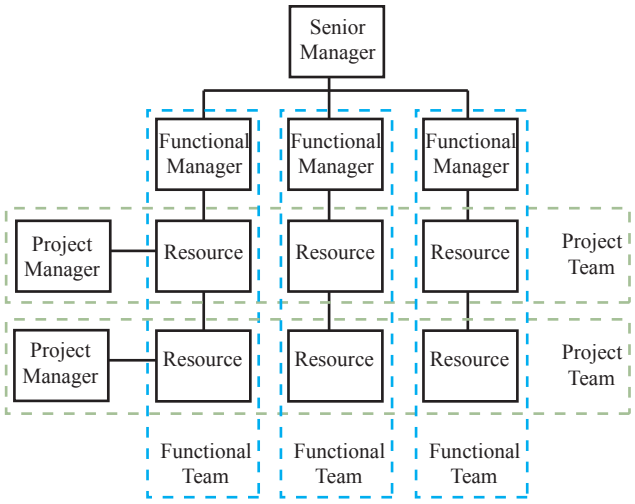
A matrix structure is an amalgam of a functional and a project structure (see figure 2.2(c)). It includes cross-functional project teams in addition to the basic functional structure. This structure introduces new cross functional communication lines within the company, and expertise can be shared from different departments to innovate new projects. This type of structure can have potential problems with



(a) Pure functional structure.



(b) Pure project structure.



(c) Matrix structure.

Figure 2.2: Different types of company structure. The connections in the diagrams indicate where there is a line of communication.

conflict as an employee might have two managers, functional and project, that they are accountable to.

A new type of structure, Virtual Teams, has also emerged recently. This structure takes advantage of IT to connect people and organisations rather than physically locating them together. While based at Motorola NCSG, I was part of a virtual team that used such a structure. The team was built up of two functional units (functional verification, and layout and floorplanning) working together on *taping out* chip designs. The entire project team was split across three sites in Scotland, England and France, with each location housing smaller teams of engineers of both functional type. Each site had a line manager, and additionally each function had a manager. So, in my case, my functional manager was located at a different site, but my line manager was at my location. To help with this the functional managers would visit the other sites regularly, and during critical points in the product development. However, we did not often physically meet with the team members at the other sites. To aid with team cohesion, and progress reporting, weekly meetings were held. This involved all team members joining a conference call and reporting progress. Additionally, *Powerpoint* presentations would be broadcast to all locations during the conference call so the entire team could see the same information. The use of email in this type of project is essential. However, the amount of email traffic increases significantly compared to when staff are located together and filtering relevant information can be time consuming.

Virtual or geographically distributed teams can also be found in academia. One example of a multi-site, multi-functional project that I have worked on is the nanoCMOS project shown in figure 2.3 (more information on this project is available at http://www.nanocmos.ac.uk/index.php). Academic projects are true projects in the way that the budget and length of the project are strictly fixed from the outset, based on the grant which has been attained to fund the project. However, this project also had matrix like properties: The project leader was also a functional manager of one of the sub-teams at one of the locations, and people reported both directly to the project leader and to their own functional manager (Principal Investigator or Co-Investigator in this case). Students are additionally supported by the Research Assistants in the project through mentoring, and training and development. Again in this case regular meetings and conference calls are a key part of

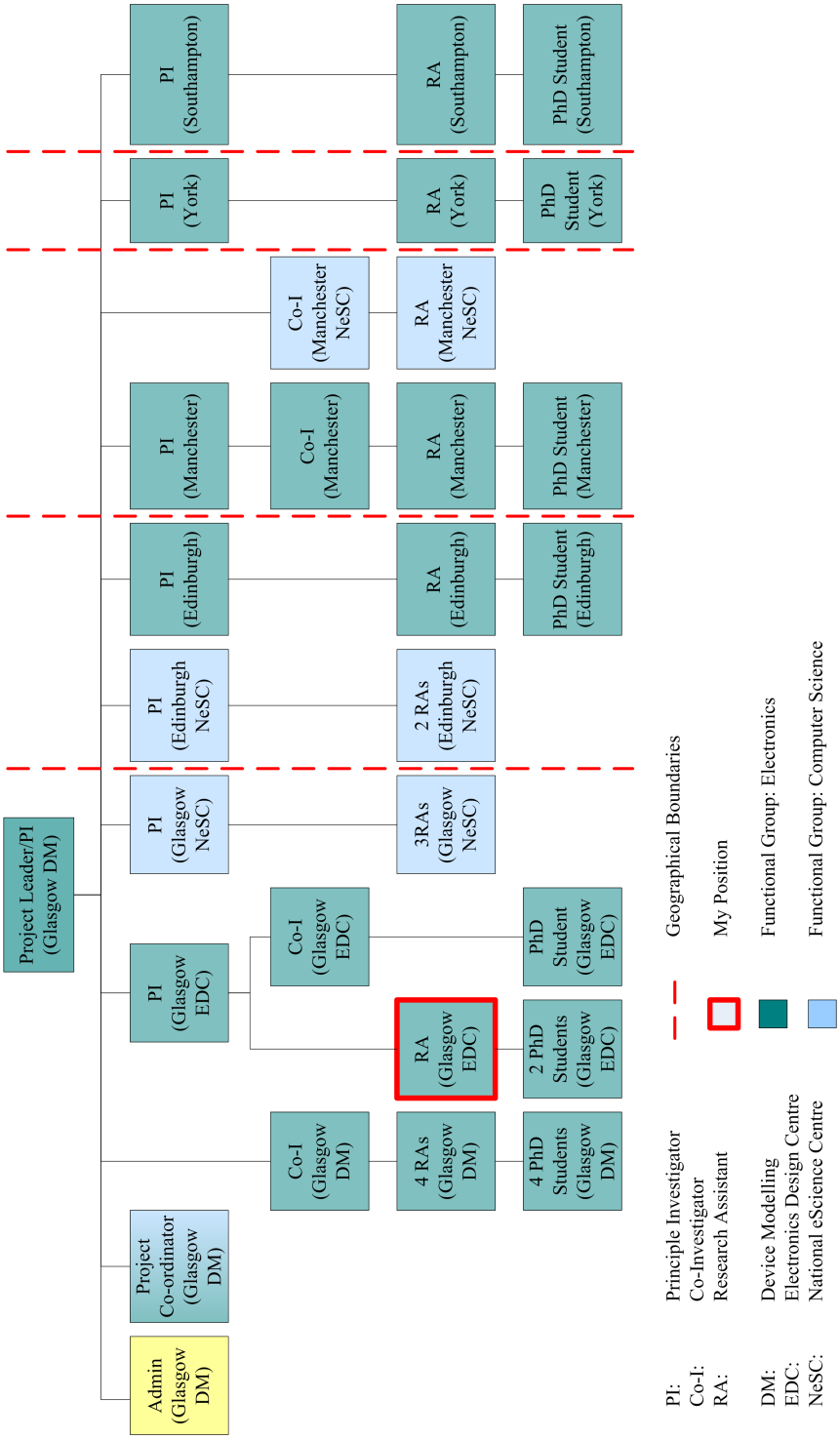


Figure 2.3: nanoCMOS. An example of a multi-functional, multi-site project.

bridging the geographical boundaries. Email is again heavily used to share information, however in this case the project web page and *wiki*[1] also played a significant part. Additionally in this case quarterly review meetings took place, where the entire team would be physically brought together at one of the sites involved in the project. Among others one of the aims of this project was to develop computing grid technologies so that people from each of these sites could make use of each others computing resources. Therefore by it's nature it is attempting to aid collaborative, data intense, multi-site technical work.

Virtual teams are now being used in many different industries. One example of a very successful virtual team was in the Russian special effects industry. To produce the films Nightwatch (Nochnoy Dozor, 2004) and Daywatch (Dnevnoy Dozor, 2006) 17 special effects companies across Russia collaborated to create the effects for the films [14].

In these examples the virtual teams were successful enterprises, however there are potential problems associated with this type of team infrastructure. It can be expensive to set up this type of team due to the additional IT costs and the potential travel expenses. There can also be frustrating problems with the additional IT required since, for example, connections can be lost mid-meeting interrupting the flow of work. Forming and maintaining a good cohesive team, as will be described in section 2.5, can be difficult as it may be difficult to instill the same kind of team spirit as a geographically grouped team. Part of the success in the examples could be attributed to the fact that they were not entirely virtual, as there were still small localised teams. Managers of virtual teams will need to be aware of the potential problems this type of structure. They will also need to be aware that controlling a project with a virtual team may be a more challenging task than if team were geographically grouped.

From my own experiences it is key that, if possible, members of a geographically distributed project team are physically brought together at important junctures in the project. At a minimum, this would happen at the stage where the project starts and the team is formed. This will help to affirm team morale and dependency forming, more so than any number of emails and structural diagrams ever can.

[1]Software that allows registered users to collaboratively create, edit, link, and organize the content of a website.

2.5 Effective Teams

Effective working teams are an essential part of all types of organisation. Whether the team is for a finite project or for a functional unit within an organisation it is essential to consider such issues as the personality make up of the group, motivational issues and stress and wellbeing in the workplace. These issues are often considered secondary to an individuals functional role in a company but are essential for an effective and high performance working environment.

There are many key things to consider when choosing a group of individuals to work in a team together, or indeed to understand how an existing team operates. If a group is to work effectively together it is important to consider the mix of personality types in the team. A successful team will include a mixture of different types, not all of which would naturally get on together on an individual basis, however collectively they make a dynamic and successful working group.

In any particular profession it is common for there to be similar personality types. In an electronics and electrical engineering environment, for example, the balance of personality types often leans towards introvert, rather than extrovert, with most having an analytical nature. A group of engineers will usually have an excellent knowledge base and people who are good at reliably completing projects - both necessary skills in that profession. However, this can mean that the team can lack some of the more people-oriented team workers and coordinators that are necessary for a good collaborative environment. These people-oriented personality types are good at encouraging team discussions, diplomacy and helping the other personality types work together effectively.

This is only one example of a potentially unbalanced team. Another example of an unbalanced team would be recruitment consultants, who generally have extroverted and reactive personalities. This again may provide the core skills required in that team, but leave it lacking in other areas. They will be good at communicating and finding new resources. However, this can leave a team lacking necessary administration and reporting skills, that are often seen as boring and of a lower priority.

Once a balanced group of individuals has been identified to work together, by a project manager for example, there are four development stages that a team will

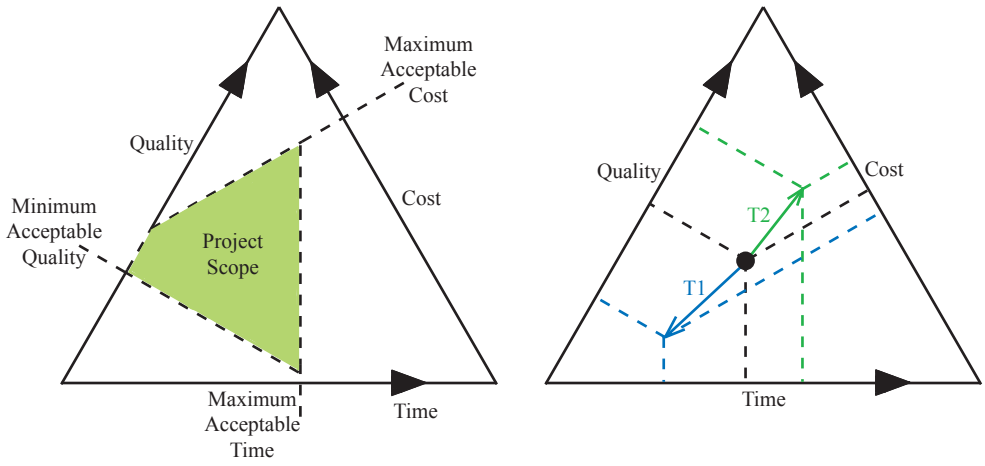
go through during the project; *forming*, *storming*, *norming* and *performing* [15]. Forming will see the group brought together. The storming stage will be where issues of conflict management and leadership will be addressed. During norming the development of team cohesion and loyalties can be observed. Finally, once the team is performing it will be effectively solving any conflict issues that arise and there will be a good collaborative approach to problem solving. There is a potential fifth stage of team development, *adjourning* or *mourning* [16]. This will occur when a team has finished working together, perhaps unsuccessfully.

As mentioned in section 2.4, in the case of a virtual or geographically distributed team these development stages can be slightly more challenging to manage, and the feeling of team loyalty and cohesion can be much more difficult to instill. Bringing the team physically together during the first three stages (forming, storming, norming) can help expediate the team to performing well together. However, this will inevitably take slightly longer than a team that is geographically grouped.

In the case of the Motorola example the team did in fact reach the fifth stage, adjourning. Where the product was successfully taped out (details in appendix A), however this also coincided with redundancies. The effects of such redundancies will be discussed in section 2.7. In this case despite the knowledge of the pending redundancies, as the team was so well established and performing well, the product was successfully completed. Rather than selective redundancies and re-employment opportunities, as the entire division was made redundant, so was this entire team. This provided an unusual situation for the functional and line managers as they too were being made redundant, but still had to go through the consultation process with their employees.

2.6 Project Planning

When planning a project it is key that a *project scope* is initially established, as illustrated in figure 2.4(a). The project scope will identify limits of time, cost and quality that are acceptable for the project. On completion of a project it's success will mainly be judged on whether or not the end result falls within the agreed scope. Any changes in where the project sits in the time-cost-quality continuum should ideally occur within the agreed project scope, however this is not always possible as



(a) Identifying project scope.

(b) An example of movement within the time-cost-quality continuum.

Figure 2.4: The time-cost-quality continuum.

often original plans and expectations can be unrealistic.

Examples of how the operating point of a project might change are shown in figure 2.4(b). In transition T1, a reduction in budget and the time allowed for the project has meant a necessary drop in the quality of the product. In transition T2, perhaps regulations on the standard of quality of the product have changed and therefore the quality requirements are greater. The time is now pushed to the maximum allowed limit to allow for this change, and a rise in cost in incurred.

Careful and realistic planning for a project is essential, as many projects fail to achieve their objectives. Planning will occur all through the project as unforeseen circumstances must be dealt with, however the cost of implementing changes in a project will increase through it's life cycle. Sources of information when planning a project will include; technical factors, company strategy, product standards, contracts, knowledge and experience, and historical data.

From my experience some of the key points in planning a successful project are the following. First, the budget plan must be realistic and include a contingency fund. The contingency fund is critical especially for long projects lasting several months, or even years, as the longer the project the more likely that prices and suppliers etc may change due to unforeseen circumstances. Building in this flex-

ibility will make implementing any necessary changes to the original plan easier. Similarly, the time plan must contain contingency or slippage allowance. Finally, when planning a project, carefully deciding who will be a part of the project team is important. The points discussed in section 2.5 are essential to this.

2.7 Restructuring and Redundancy

Restructuring within an organisation can be necessary for many reasons and it's effects can be far reaching. The principle reason for any company's structural change is usually profitability. This may take the form of improving efficiency within the company, spinning out part of the company, or downsizing due to an economic downturn. In all of these cases information in the form of financial and management accounting reports will have been key in making decisions. Financial reports such as profit and loss accounts, balance sheets, and cash flow statements will give a historical basis for decisions. Whereas, management reports will give predictions on future budgets and performance.

If a company decides to restructure to improve efficiency within the organisation it may be due to a change in the management philosophy. Perhaps a change from a traditional functional structure (see figure 2.2(a)) to a more dynamic structure such as matrix (see figure 2.2(c)).

In some cases if a department or devision is not performing well it is not uncommon for a company to make it redundant. The financial accounting reports may show that the department is suffering from ongoing losses, and perhaps the management accounting reports indicate that this may not be envisaged to improve.

The case of spinning out part of a company is usually more optimistic, such as that described in Mototola's 2003 press release when they decided to spin out their semiconductor products sector (eventually to become Freescale Semiconductor) [17]. They believed that the semiconductor industry was on the up and that there was potential for this sector to perform well as an independent company, which has since proved to be the case. Unfortunately, as mentioned in section 2.2, there were necessary redundancies on this occasion, which is often the case when a large company decides to do restructuring on this scale.

In a situation where employees suspect that redundancies might be made they

will find their job security threatened, but not necessarily their employment security. Job security relates specifically to an employees position in a particular company, whereas employment security more generally relates to a persons employability within their particular industry. Employment security can be gained or improved by a person maintaining a broad spectrum of experience and knowledge and maintaining a self-reliant and versatile attitude towards work. Employees who do not strive to create their own sense of employment security are far more likely to suffer stress should the threat of redundancies occur.

2.8 Continuing Professional Development

In addition to the academic advancement gained, in both technical and business topics, continuing professional development was also considered and important factor in achieving the the EngD. Some of the events and training courses that were attended are listed below. In addition to these, I presented my work regularly during meetings and seminars at the University of Glasgow. During numerous conferences, tutorial sessions were attended that either related directly to my research, or to further my knowledge more generally of new techniques and advancements in semiconductor research. I have been a member of the Institute of Electrical and Electronics Engineers (IEEE) since commencing the EngD, initially as a student member, and now as a full member.

- Annual EngD training/team building events, organised by the Institute for System Level Integration, Livingston, Scotland.
- Workshop on EDA tools and design flows for Microelectronics design by Microelectronics Support Centre at STFC Rutherford Appleton Laboratory, 2003, Edinburgh, Scotland.
- International Symposium on Circuits and Systems (ISCAS), 2004, Vancouver, Canada.
- Grad School, 2005, Brighton, England.
- International Symposium on Circuits and Systems (ISCAS), 2006, Kos, Greece.

- Conference on Optoelectronic and Microelectronic Materials and Devices (COMMAD), 2006, Perth, Australia (paper presented).
- Mathematica training course, 2008, Glasgow, Scotland.
- UK Design Forum (UKDF), 2008, Manchester, England.
- Cadence CDN Live, 2008, Munich, Germany.
- Matlab training course, 2008, Dundee, Scotland.

2.9 Summary

In this chapter the necessary redirection of my research topic has been discussed. Thus, presenting a pertinent example of restructuring and redundancies in the global electronics industry. The industrial context of GaAs MOSFET research has been presented, along with the main companies working in this area.

Relevant points from the business and management modules studied have been discussed, particularly those relevant to my own experiences. Examples of management structures in industry and academia have been examined, especially with reference to geographically distributed teams, which presents new challenges in logistics and team dynamics. Issues with effective and balances teams have been presented, with particular reference to the types of personality that might be typically be found in an engineering environment. Key aspects of project planning have also been discussed. The reasons for, and effects of, restructuring and redundancies were further explored with reference to stress, job security, and employment security.

3 Literature Review & Background

3.1 Introduction

For over 40 years researchers have been looking into potential GaAs MOSFET devices [18]. During this time many significant advances in both GaAs and other semiconductor devices have taken place. The most significant obstacle in developing GaAs MOSFETs over the years has been in finding a suitable gate oxide for use with GaAs devices. Due to this, development in GaAs technology (and other III-V materials) for a long time continued in the direction of HEMT-like structures and other devices [3].

In this chapter I shall first look at semiconductor development generally. Then I shall examine some of what I consider to be the most significant steps in the advancement towards realising a feasible enhancement-mode GaAs MOSFET technology and the issues associated with this. In particular issues such as gate oxides

for GaAs substrates, device modelling of GaAs MOSFET devices and work that has been done regarding circuit design for GaAs devices shall be discussed.

3.2 Semiconductor Development and *the Roadmap*

Since the beginning of semiconductor device development many different semiconductors materials have been investigated. Many of the first transistors were germanium based, including the first transistor built by Shockley, Bardeen and Brattain in 1947 [19, 20]. However, since Kahng and Atalla's invention of the silicon MOSFET in 1960, silicon has became the semiconductor of choice for digital circuits [19, 21]. There are several reasons for this: silicon is a cheap material with a low cost of production; it has a good native oxide in SiO_2 with which it does not generate localized interface states at the oxide/semiconductor interface; and it can be easily grown using the Czochralski or float zone technique to produce long single-crystal ingots which can be used to produce wafers for fabrication [19].

In 1965 Gordon Moore's now legendary analysis of growth in the semiconductor industry, based on the number of components per integrated function, gave the first indication of what the industry could expect to achieve with succeeding generations of electronics [22]. He initially estimated that the number of components on an integrated circuit would double every year. Moore also noted in this paper that *"Silicon is likely to remain the basic material, although others will be of use in specific applications. For example, gallium arsenide will be important in integrated microwave functions. But silicon will predominate at lower frequencies because of the technology which has already evolved around it and its oxide, and because it is an abundant and relatively inexpensive starting material."* Since 1965 the number of components on an integrated circuit has continued to double every 1.6 years, close to Moore's original estimates [23].

The realised trend predicted by Moore is now formalised in the International Technology Roadmap for Semiconductors (ITRS). First published in 1994 the ITRS sets out to predict where the industry both expects to be and where it should aim to be over the next 15 years. Every two years a revised edition of this is released, with an update with more minor revisions being released in the intermediate years. It is now widely recognised that to maintain growth at the historical rate it will be

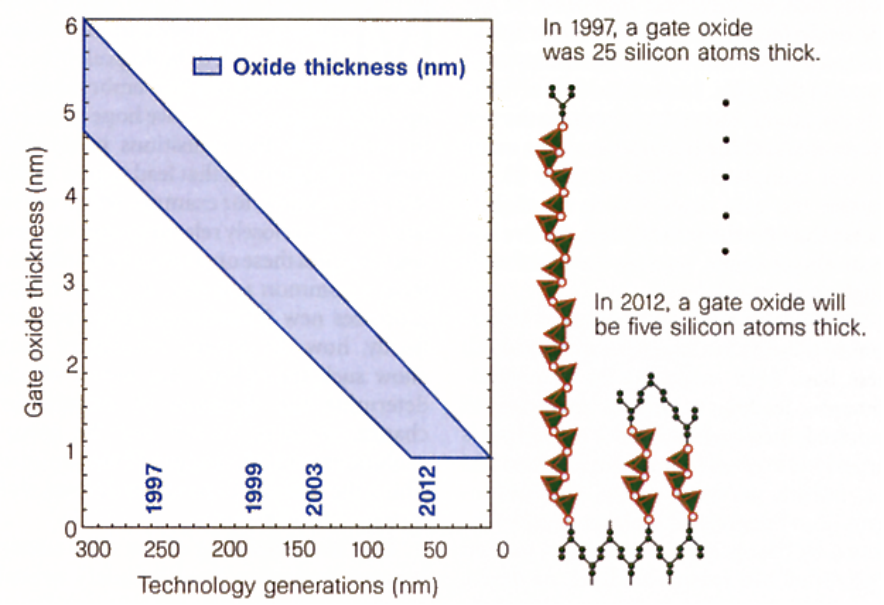


Figure 3.1: Semiconductor Industry Roadmap [1].

necessary to include novel device structures and new materials beyond traditional silicon CMOS devices.

This trend for the ITRS to look beyond silicon to new emerging devices has come about due to the fast approaching physical limits of traditional CMOS Si/SiO_2 devices. With device scaling the thickness of the SiO_2 gate oxide layer is now at an atomic scale. It is predicted that by 2012 the gate oxide layer in these devices will only be 5 atoms thick (see figure 3.1) - at 4 atoms (0.7 nm) the electrical insulation of the gate oxide breaks down [24].

There has already been a great deal of effort in moving toward solving this problem. Silicon CMOS devices have been demonstrated with gate lengths as small as 15 nm. However, to fabricate these nano-scale devices, unconventional gate dielectrics are required [25]. Yu *et al.* used a nitride/oxynitride dielectric structure to achieve this in their work. The gate dielectric was 1.4 nm thick with an equivalent oxide thickness of 0.8 nm, implying a dielectric constant of 6.8 (SiO_2 is only 3.9). The use of a high-κ dielectrics, to make ultra-short gate length MOSFETs, is one of the many methods which have been put forward as a potential solution to the scaling problem, and it is anticipated that even higher-κ dielectrics will be required

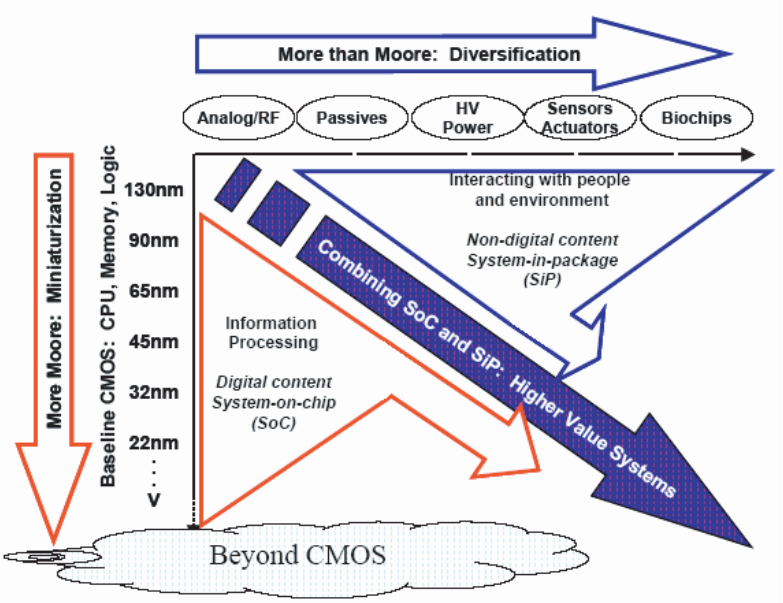


Figure 3.2: The future of semiconductor systems [2].

to meet future targets. In addition to the use of high-κ dielectrics, some of the novel device structures that are expected to be important in looking beyond the limits of conventional CMOS scaling include; ultra-thin body, silicon-on-insulator, strained silicon, multiple-gate MOSFET and III-V structures [11, 26].

Another factor to consider for future devices, in addition to the continued scaling of silicon and new emerging devices, is that there is likely to be a continuation of the trend toward system-on-chip and system-in-package. This will mean increased complexity and functionality within single systems. Figure 3.2 illustrates where the ITRS roapmap places these in the future of semiconductor development.

The realisation of GaAs MOSFETs for digital design presents potential new integration possibilities for future circuits and systems, due to already existing RF and optoelectronic GaAs devices, as discussed in section 2.3.1.

3.3 GaAs MOSFET Device Development

The original development of III-V devices naturally lagged slightly behind that of silicon as the properties of silicon had been widely studied since 1940, but it wasn't

until 1952 that Welker identified III-Vs as semiconductors [19, 27].

As far back as 1965 GaAs MOSFETs were being explored using SiO_2 as the gate dielectric, however device results published between 1965 and 1989 did not meet expectations [18, 28–33]. A major contributer to this was that a key problem hindered the development of GaAs MOSFET devices: the lack of a suitable gate oxide. The oxide issue brought with it problems associated with the density of states and Fermi level pinning at the oxide semiconductor interface [34]. A more detailed account of the developments of oxides for these devices will be given in section 3.4 as this in itself is an extensive and well researched area. As a consequence of this, little was published on GaAs MOSFETs again until 1996 when Ga_2O_3 emerged as a suitable gate oxide. Thus, silicon dominated the market for digital devices, and GaAs devices were generally seen as a smaller specialist market mainly for microwave applications.

There are some issues associated with producing GaAs devices that need to be considered when looking towards large scale production and the production of complex IC's. For example, GaAs is a more brittle substrate than silicon and has a lower thermal conductivity (0.46 W/cm°C compared to 1.31 W/cm°C for silicon). Therefore, in complex IC's careful consideration of power consumption, power distribution and heating of substrates may be necessary. One possibility that may help to avoid the brittle substrate issue is that GaAs can be grown on a silicon substrate. This will be discussed further in section 3.6.

Many of the initial companies and institutes that investigated GaAs MOSFETs did not continue work in this area [18, 28–33]. For example, due to the problems with suitable gate oxides for GaAs MOSFETs, Mimura *et al.* at Fujitsu eventually decided to take research in another direction and later in 1979 Mimura submitted a patent for the first HEMT device [35]. Figure 3.3 shows a sketch by one of Mimura's colleagues of both a GaAs MOSFET and a GaAs HEMT. As we shall see, the work that followed in HEMT technology would later be of great benefit to GaAs MOSFET designers.

Once Passlack *et al.* had solved most of the oxide issues for GaAs MOS devices in 1996, Ren *et al.* and Wang *et al.* built on this and went on to publish work on GaAs/Ga_2O_3 MOSFET devices [36, 37]. They showed that functioning PMOS and NMOS devices could be made using Passlack's oxide methods .

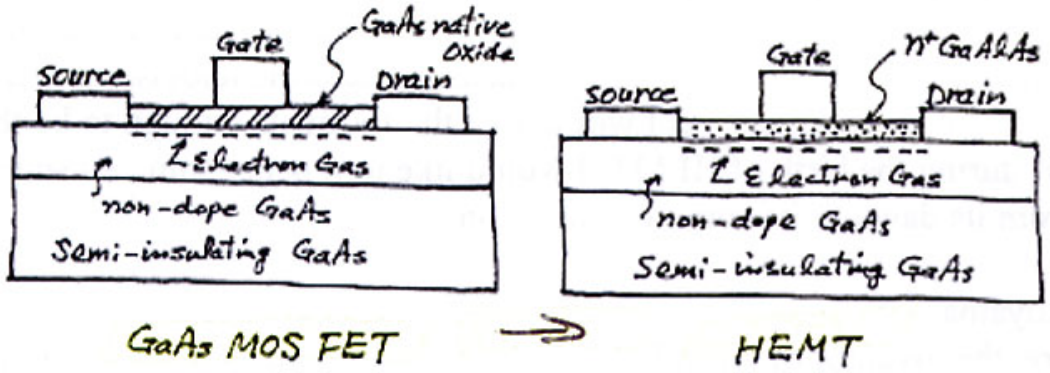
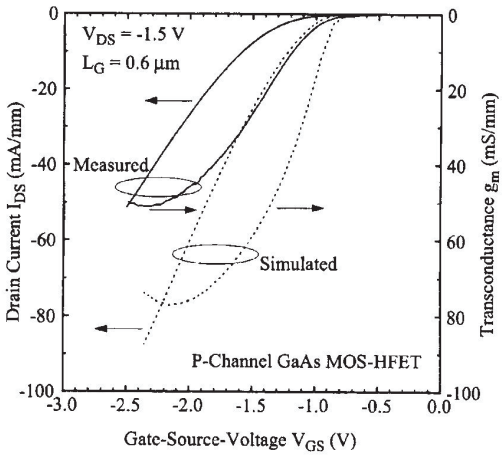


Figure 3.3: Diagram showing the structural comparison of a GaAs MOSFET and HEMT by Masumi Fukuta [3].

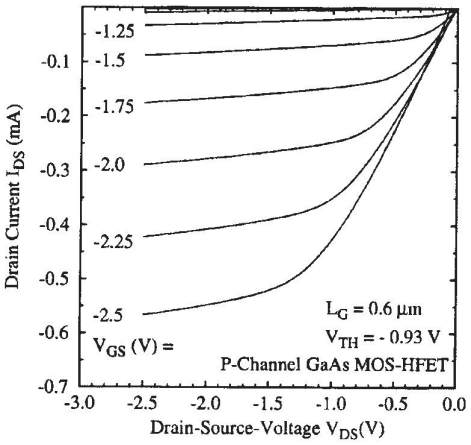
In 2000, heterostructure gate stacks started to be used in GaAs MOSFET devices and full advantage of the potentially higher mobility in GaAs MOSFET devices could finally be taken. The gate stack of a device is the cross section of materials used from the top to the bottom of the device, through the centre of the gate. A heterostructure gate stack contains multiple layers of different materials below the oxide. Heterostructure devices which have a GaAs/InGaAs layer structure are naturally strained due to the slight lattice mismatch between the different materials. This effect causes the thiner layer to stretch to the line up with the other material, therefore creating a strained layer in the device. Materials which express this property are known as pseudomorphic. Pseudomorphic InGaAs channels grown on GaAs substrates have been shown to be the primary reason for the excellent performance observed in PHEMTs due to the superior transport properties of the electrons. This technique has now been applied to GaAs MOSFET structures [38]. By introducing strain into devices in this way can improve the drive current observed.

The key developments were now in place for high performance digital GaAs MOSFETs to be successfully developed - a good oxide/semiconductor interface and a high electron mobility channel. From here on GaAs MOSFETs technically became MOSHFETs or MOSHEMTs, but I shall continue to use MOSFET for consistency.

In 2002 I-V characteristics of a GaAs enhancement mode MOSFET using a Ga_2O_3 gate oxide were published by Passlack *et al.* as shown in figure 3.4 [4]. This presented characteristics of a p-channel MOSFET with a gate length of 0.6 μm and



(a) PMOS gate characteristics and transconductance.



(b) PMOS drain characteristics.

Figure 3.4: Device characteristics as published by Passlack *et al.* [4].

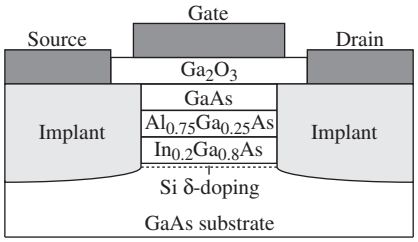


Figure 3.5: Cross-section through the structure of a GaAs MOS transistor. Based on the structure demonstrated by Passlack *et al.*.

width of 10 μm. The gate oxide had a dielectric constant of 10 and was deposited using Motorola's patented method published in 2000, which will be discussed in section 3.4 [39]. A diagram of the device structure is shown in figure 3.5. When the research presented in this thesis was started this was the most up to date information regarding enhancement-mode GaAs MOSFETs (being the most pertinent type of device for digital circuit design).

Since then Motorola (now Freescale) have patented the GaAs MOSFET technology that they developed, and continued to work towards improving the characteristics of these devices [40–42]. Recent published work, again by Passlack *et al.*, showed that devices have now been demonstrated with even higher-κ dielectrics ($\kappa \cong 20$), however no device dimensions were given [5]. This time the devices were

enhancement-mode NMOSFETs and mobilities were found to exceed 6000 cm^2/Vs. The gate stack demonstrated is illustrated in figure 3.6 and follows on from that which was demonstrated previously by Passlack.

Further work, in collaboration with the University of Glasgow, has continued on these devices and good characteristics have been demonstrated for GaAs NMOS devices with a 1 μm gate length [43–45]. Threshold voltages have been reduced (< 0.3 V), drive currents have been improved (≈ 400 $\mu A/\mu m$), mobility has been increased (> 5000 cm^2/Vs), and contact and sheet resistances have been reduced. Steps to scale these devices are being made, however this currently only includes lateral scaling down to 0.3 μm gate length devices.

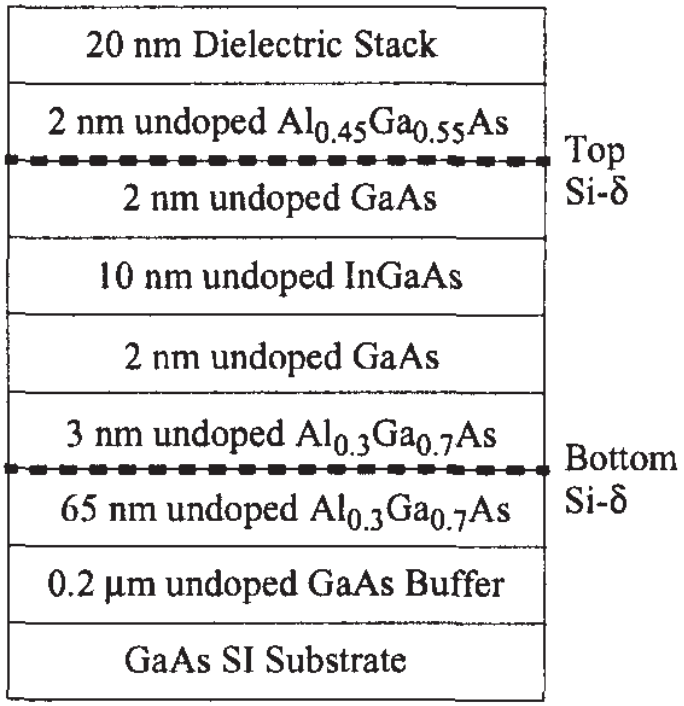


Figure 3.6: Gate stack demonstrated in ref. [5].

Since 2002 Passlack *et al.* at Motorola/Freescale, along with collaborators at the University of Glasgow, have dominated in work done on enhancement-mode GaAs MOSFETs. However, there has also been work published by Agere Systems regarding depletion-mode GaAs MOSFETs. Ye *et al.* have looked at using Al_2O_3 as the gate dielectric [46–49], and Yang *et al.* have explored $Ga_2O_3(Gd_2O_3)$ [50, 51].

In addition to the device development discussed above there has also been work done on modelling of the potential performance of GaAs MOSFET devices. See section 3.5 for more detail.

3.4 The Search for a Suitable Gate Oxide for GaAs MOSFETs

Since researchers began looking at GaAs as a potential material for MOSFETs the same problem has come up time and time again; which gate oxide is the most suitable to use? This problem has been explored by looking at different oxide materials. However, in some cases research was abandoned in this area and taken in the direction of HEMT technology [3, 52]. Some of the oxides which have been explored are Si_3N_4, SiO_x, Al_2O_3, and Ga_2O_x [53].

As mentioned previously, the the main problem associated with finding a suitable oxide was the density of states and Fermi level pinning at the oxide/semiconductor interface. Fermi level pinning can be caused when there is a very high density of states at the oxide/semiconductor interface. Interface states are electronic states that occur due to the termination of a periodic lattice structure at a surface, they can occur due to lattice defects or free bonding sites. Ideally the density of interface states needs to be below, or of the order of, 10^{11} $eV^{-1}cm^{-2}$ to prevent Fermi level pinning [54, 55]. If the density of interface states is greater than this, then the Fermi level becomes fixed close to the charge neutrality level, regardless of the semiconductor doping level or type [56]. The charge neutrality level is the Fermi level of the equivalent undoped semiconductor. When this happens there will be no electron accumulation or inversion and the MOSFET will not operate correctly. Hence, to combat this problem the key is the reduction of the density of states to an acceptable level. This was eventually achieved by careful selection of the gate oxide material and its deposition method.

In 1979 Takashi Mimura and colleagues investigated the GaAs oxide issue [52]. They developed a low-temperature plasma oxidation technique to grow a stoichiometric native oxide of GaAs. However they found that no electron inversion or accumulation was possible due to the large density of interface surface states cap-

turing electrons.

Eventually in 1989 it was shown that the interface state density could be reduced to an acceptable level ($\approx 10^{11}$ $eV^{-1}cm^{-2}$) and the Fermi level at the oxide/semiconductor interface could be unpinned [34]. This was achieved by using a H_2 surface plasma treatment followed by a N_2 plasma treatment at 200 °C prior to the oxide deposition. The oxide was reactively deposited *in situ* by electron beam evaporation of Ga onto the substrate placed in an O_2 RF plasma. This was the first step toward a successful oxide/semiconductor interface for an enhancement-mode GaAs MOSFET. However, further improvements in the quality of the oxide were still necessary for the fabrication of devices due to problems with leakage current. Also the dielectric properties of the oxide were not ideal.

From this point onwards work by Passlack and colleagues first at AT&T Bell Laboratories and then at Motorola Inc. dominated the field [53, 54, 57–59]. They used a new method for depositing an oxide on GaAs using a $Gd_3Ga_5O_{12}$ high purity crystal as the source for the oxide deposition, as opposed to the O_2 RF plasma method. During heating the crystal slowly releases high purity Ga_2O_3 which in turn deposits a high quality dielectric Ga_2O_3 film on the substrate. In addition to the producing a low density of states, this method had the advantage of giving a static dielectric constant of between 9.9 and 10.2 for the Ga_2O_3 films, and of giving planar surfaces both at the oxide/semiconductor interface and at the surface of the oxide on a nanometer scale [53]. Planar surfaces are especially important for optoelectronic devices, hence along with moving towards suitable gate dielectrics for GaAs digital logic, the same oxide films could be successfully used for optoeletronics applications. Suitable optical properties, such as the index of refraction, of thin film Ga_2O_3 also play an important factor in it's suitability for optoelectronic devices [54].

Since 1996 Ga_2O_3 has dominated as the gate oxide of choice for enhancement-mode GaAs MOSFETs, with Al_2O_3 being a popular choice for depletion-mode devices.

Following two key patents by Motorola in the United States in 2000 and 2002 [39, 60] that concerned oxide/semiconductor interfaces for III-V devices, the oxide problem for GaAs was effectively solved. Methods were now in place to fabricate a high-purity gate oxide with an atomically abrupt oxide/semiconductor interface on a GaAs substrate, with a surface roughness on the scale of 0.2 - 0.3 nm (see

figure 3.7). This deposition was carried out using an effusive evaporation method from crystalline Ga_2O_3 under ultrahigh vacuum conditions to form a Ga_2O_3 gate oxide [6, 39, 61]. A result from using this method is shown in figures 3.4 and 3.5.

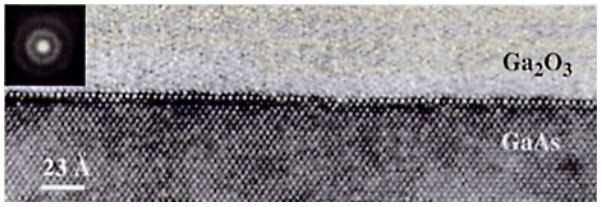


Figure 3.7: Transmission electron micrograph of the oxide/semiconductor interface made by Yu *et al.* at Motorola [6].

3.5 Device Modelling of GaAs MOSFETs

There are several device modelling papers of notable interest in the field of GaAs MOSFETs. Particularly work done by Karol Kalna and colleagues at the University of Glasgow using Monte Carlo techniques [62–65]. These papers illustrate the potential performance of devices with gates lengths ≤ 100 nm. They do not however include a comparison with manufactured GaAs MOSFET device characteristics. This is due to the fact that there are two key times in the new device-to-market cycle when device modelling plays a significant part, as illustrated in figure 3.8. The first is, as Kalna's work, to look at potential devices using knowledge of the materials and well calibrated physics based custom modelling tools [65] (stage 2 in figure 3.8). The second comes once successful devices have been manufactured and characterised, in this case measured results of a fabricated device are used as an additional method of calibration (stages 5 and 6 in figure 3.8). Once compact models have been created circuit designers can then use these to design manufacturable circuits in a particular technology. The goal of this research was to complete this second modelling stage and use the results to investigate circuit design and performance. Chapters 4, 5, and 6 cover stages 5, 6, and 7 of figure 3.8 respectively.

Most of the work by Kalna in this area has been published since 2002. However, back in 1989, Fischetti and Laux at the IBM Research Division of the T. J. Watson Research Center also looked at modelling in this area [66]. Their results

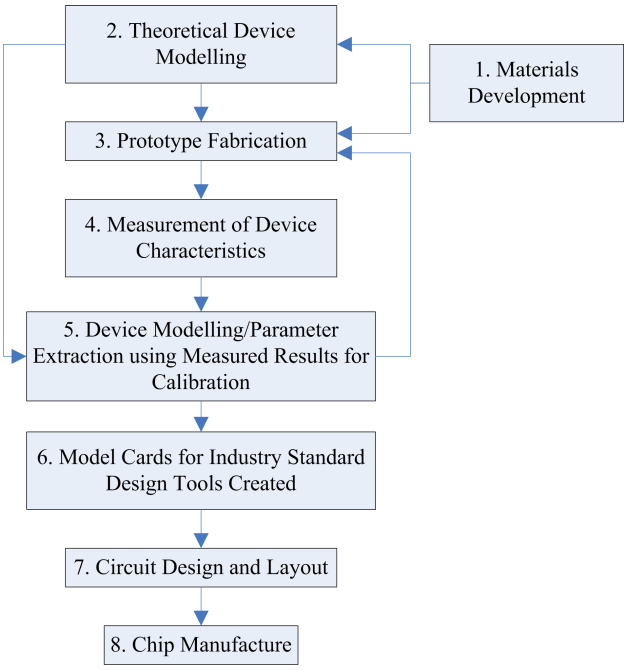


Figure 3.8: New device-to-market design flow.

where disappointingly pessimistic, this was partly due to the assumptions that they made about their GaAs devices. They assumed that a GaAs MOSFET would essentially be identical to the structure of a silicon MOSFET, so no heterostructure layers were included, and a SiO_2 oxide was assumed as this was before a good oxide/semiconductor interface specifically for GaAs had been established (see section 3.4).

Kalna *et al.*'s results showed a more optimistic future for GaAs MOSFETs as they typically included a heterostructure-like structure with an InGaAs channel. They showed that 80 nm InGaAs-channel GaAs MOSFETs could outperform equivalent silicon MOSFETs by up to 200% by increasing the source/drain doping to the maximum physically possibly for GaAs, 5×10^{19} cm^{-3} (2×10^{19} cm^{-3} is more realistic for that which can be achieved by current technology [64]). However at a gate length of 35nm the GaAs devices were shown to be no better than strained silicon devices [64]. Details of the thicknesses of layers in the gate stack and the dielectric constant of the oxide were not given in this work.

Other recent work by Kalna *et al.* showed the relative improvements of scaling a

heterostructure GaAs MOSFET device from 100 nm to 70 nm and then to 50 nm, drain currents were found to improve by 60% and 90% respectively. Full details of the gate stack layer structure were given however no details of the source/drain doping used were given [65].

Most recently, Monte Carlo modelling results have been published of 30 nm, 20 nm, and 15 nm heterostructure MOSFETs, again showing optimistic results [67]. The simulations have been calibrated against against electron mobility and sheet density measurements from fabricated III-V MOSFET structures with a high-κ dielectric. However, these devices do not include the effects of contact resistance, which can have a substantial effect on performance.

3.6 GaAs MOSFETs - Related Developments

An important development related digital GaAs is the is the possibility of creating GaAs transistors on a silicon substrate, which was the focus in research carried out by Eisenbeiser *et al.* [68] and Kalna *et al.* [62]. One of the biggest benefits of having GaAs on silicon technology is the potential to combine on a single SoC high speed III-V MOSFETs with traditional silicon CMOS blocks. Another potential benefit is that by growing GaAs on silicon any issues associated with having a brittle GaAs substrate might be avoided.

Eisenbeiser *et al.* used a crystalline $SrTiO_3$ buffer layer to grow GaAs on silicon using molecular beam epitaxy. They compared the performance of a GaAs MESFET on a GaAs substrate to one grown on a silicon substrate. They found that the device on the silicon substrate performed almost as well as the GaAs substrate device (94% of the electron mobility). Although this work was done with GaAs MESFETs the fundamental principle of growning GaAs devices on silicon equally applies to other types of GaAs device, for example MOSFETs.

The research by Kalna *et al.* looked in to the potential performance of sub-100nm n-type strained $In_{0.2}Ga_{0.8}As$ channel MOSFETS with a high-κ dielectric utilising GaAs on 12" silicon EPIGEN technology, they found that the InGaAs MOSFET had better potential for improvement with scaling compared to silicon and strained silicon technologies.

In addition to growing GaAs directly on silicon, it has been shown that the use

of a SiGe/Ge buffer can improve the lattice matching between the materials [69]. Further benefits of this, and integration possilities will be discussed in chapter 7

3.7 Circuit Design for GaAs Devices

So far there have been very few publications regarding circuit design with GaAs MOSFETs. This is mainly due to the fact that, as discussed, until recently high quality devices had not been demonstrated that would be suitable for digital circuit design.

As mentioned previously Mimura *et al.* had been looking at GaAs MOSFET devices and the associated oxide issues in the late 70's, using a plasma oxidation technique for the gate oxide [31, 32, 52]. The same group at Fujitsu also published work at that time on circuit design relating to the GaAs MOSFET devices they had developed [70, 71]. In these papers, Yokoyama *et al.* examined 13-stage enhancement-depletion and enhancement-enhancement type ring oscillators. Figure 3.9 shows the two types of inverters used to make the oscillators. When a V_{dd} of 3 V was used with the E/D inverter a voltage swing of 2.7 V and maximum transfer gain of 3 were obtained [70]. For the E/E ring oscillator the best power delay product and propagation delay achieved was 26 fJ and 385 ps respectively, the E/D oscillator achieved 2 pJ and 110 ps. These figures were obtained at a V_{dd} of 8 V.

In 2000 Hong *et al.* (at Bell Laboratories, Lucent Technologies) published the only results to date showing circuits using GaAs/Ga_2O_3 CMOS technology [72]. They presented a CMOS inverter and a PMOSFET resistive inverter for comparison to demonstrate that their GaAs process could be used to create functioning CMOS logic. The oxide deposition method used was using a $Gd_3Ga_5O_{12}$ single crystal source, previously described. The dimensions of the transistors used in the CMOS circuit are shown in figure 3.10, V_{dd} was 1 V and full voltage swing achieved as expected. These sizes were chosen to ensure that the transconductances of the two devices were equal. Unfortunately the devices that they fabricated were far from ideal and they only exhibited an effective electron mobility of 470 cm^2/Vs (the electron mobility in undoped GaAs is 8500 cm^2/Vs, and 1450 cm^2/Vs in silicon) in the n-channel device, which they attributed to the implant activation process and the parasitic resistance [73].

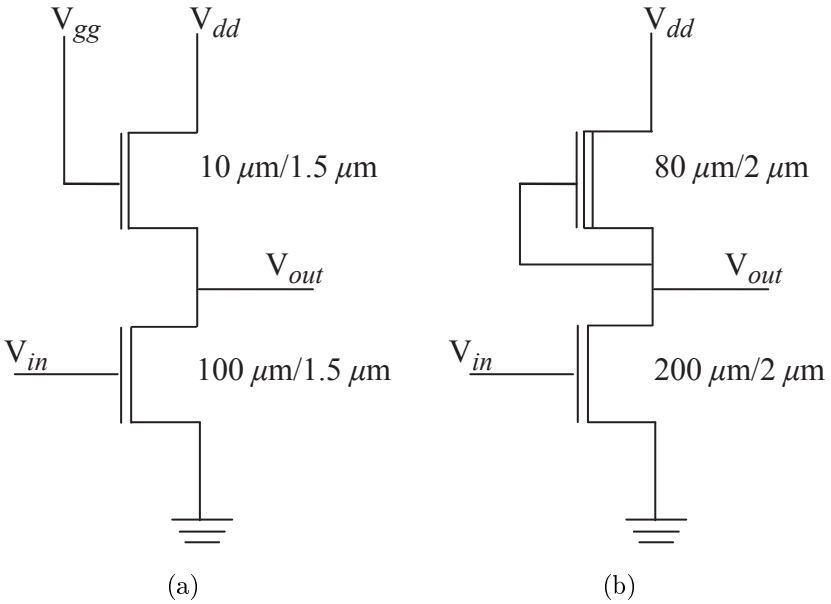


Figure 3.9: Inverter styles used in the 13-stage ring oscillators explored by Yokoyama *et al.*. (a) Enhancement load NMOS inverter. (b) Enhancement-depletion directly coupled FET logic.

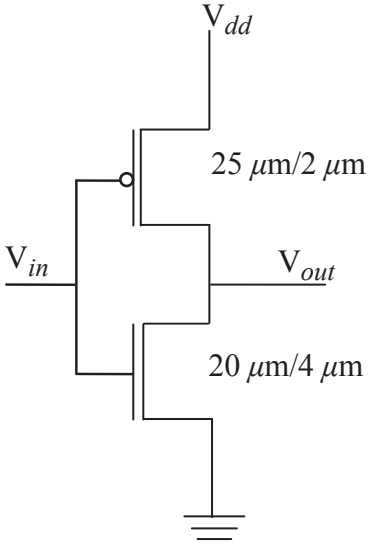


Figure 3.10: CMOS inverter circuit with transistor dimensions, used by Hong *et al.*.

With recent advancements in GaAs/Ga_2O_3 MOSFET technology it is anticipated that more work in this area will be published, which will hopefully better reflect the results that have been seen with individual device fabrication.

In chapter 6 an analysis of different digital circuit styles will be given along with a discussion of the appropriateness of these to GaAs digital design. In particular three logics styles will be explored: CMOS, NMOS precharge, and saturated enhancement load NMOS.

3.8 Summary

Digital GaAs MOSFETs are now seen as a potential enabling technology to help deal with some of the ITRS's future technology requirements. Particularly, the potential for full system integration with RF and optoelectronic components is an attractive feature of these devices.

Two key developments have enabled the successful development of GaAs MOSFETs; extensive work on finding a suitable gate oxide in Ga_2O_3 and the use of a heterostructure structure to take full advantage of the transport properties of GaAs and it's compounds.

Currently Freescale and Agere Systems (now LSI) are leading the development in GaAs devices for digital applications. However this is not entirely surprising when the movement of key researchers between companies is examined. For example, as discussed a great deal of the important enabling research in to oxides for GaAs was done at AT&T Bell Laboratories who at that time had Passlack, Mannaerts, Hong and Chu as part of their research staff. In 1996 AT&T Bell Technologies (which included AT&T Bell Laboratories) was spun-out as Lucent Technologies. In August 2000 Agere was incorporated as a subsidiary of Lucent Technologies and then spun-off in June 2002. This is the path that Mannaerts, Hong and Chu took. Passlack's work continued at Motorola (1997) and then at Freescale (2004). Many other key researchers such as Abrokwah and Yu also moved from Motorola to Freescale at this time as Freescale was a spin-out of the Semiconductor Products Services devision of Motorola.

4 Drift-Diffusion Device Modelling & Calibration

4.1 Introduction

The keystone of this research was to create GaAs MOSFET models, based on measured device results, that could be integrated into circuit design tools. This was a two stage process involving physics based device modelling, and then the adaptation of these physical models into compact models. Compact models can be integrated

with circuit design tools, thus facilitating an investigation into the properties of GaAs devices in a circuit design context.

In this chapter the first of these two stages will be addressed, physical calibrated drift-diffusion models will be presented. In chapter 5 the second stage will be addressed where compact models are developed from the drift-diffusion results.

4.2 Design Tools - Physics and Features

The industry standard two dimensional drift-diffusion based device simulator Medici (by Synopsys) was used for all device modelling in this project. It is a flexible tool that offers many different material types for device construction. The physical characteristics of the materials can be altered should the user have more accurate data than that built into Medici. If there are materials required by the user that are not already defined then the user can define additional materials.

Medici's primary function is to solve Poisson's equation (4.1) and the current continuity equations (4.2) self-consistently for the electrostatic potential (ψ) and the electron and hole concentrations (n and p, respectively). Both Poisson's equation and the continuity equations describe the electrical behaviour of devices. Where ϵ_s is the permittivity of the semiconductor, ρ_S is the charge density, N_D^+ is the ionised impurity density of donors, N_A^- is the ionised impurity density of acceptors, q is the elementary unit of charge, U_n is the net electron recombination, U_p is the net hole recombination. In Medici ψ is always defined as the intrinsic Fermi potential.

$$\epsilon_s \nabla^2 \psi = -q\left(p - n + N_D^+ - N_A^-\right) - \rho_S \tag{4.1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla} \cdot \vec{J}_n - U_n \tag{4.2a}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\vec{\nabla} \cdot \vec{J}_p - U_p \tag{4.2b}$$

The current density components ($\vec{J}_n$, $\vec{J}_p$) of the continuity equations can be written so that the drift and diffusion components of the equations can be separated. This is shown in equation 4.3, where the $q\mu_x\vec{E}_x x$ component describes the drift and

the $qD_x\vec{\nabla}x$ component describes the diffusion. Where μ_n is electron mobility, μ_p hole mobility, ϕ_n is the quasi-Fermi potential for electrons, ϕ_p is the quasi-Fermi potential for holes and $\vec{E}_n$ and $\vec{E}_p$ are as in equation 4.4. In low electric fields the diffusion coefficients D_n and D_p can be described using the Einstein relationship shown in equation 4.5. Where k_B is Boltzman's constant and T is temperature.

$$\vec{J}_n = -q\mu_n n\vec{\nabla}\phi_n = q\mu_n\vec{E}_n n + qD_n\vec{\nabla}n \tag{4.3a}$$

$$\vec{J}_p = -q\mu_p p\vec{\nabla}\phi_p = q\mu_p\vec{E}_p p - qD_p\vec{\nabla}p \tag{4.3b}$$

$$\vec{E}_n = \vec{E}_p = E = -\vec{\nabla}\psi \tag{4.4}$$

$$D_n = \frac{\mu_n k_B T}{q} \tag{4.5a}$$

$$D_p = \frac{\mu_p k_B T}{q} \tag{4.5b}$$

The default solution method in Medici is to use equations 4.1, 4.2 and 4.3. This neglects the effects of bandgap narrowing and assumes Boltzman carrier statistics. However, the user can specify additional solution methods to help improve the accuracy of the simulations and aid the convergence of simulations. Not all of these can be selected, but rather a subset of all of the solution methods can be used. Table 4.1 shows the allowed combinations of additional mobility model solution methods, the default is to use a fixed value for the mobility. The use of these additional solution methods can improve the convergence of simulations and, more importantly, provides a more physically accurate result. The models fall into three categories; low field, transverse field and parallel field models. Only one model from each category can be used at a time, and as shown in the table some of the models span two categories thus limiting the choices available. In section 4.4.2.3 I shall discuss the solution methods from table 4.1 that I chose to use in my work. Further information about the other models, and Medici generally, can be found in the Medici user guide [10].

Table 4.1: Mobility model choices in Medici.

Low Field	Transverse Field	Parallel Field
LUCMOB		
IALMOB		
CCSMOB	HPMOB	
LSMMOB		FLDMOB
GMCMOB		TMPMOB
SHIRAMOB		
ANALYTIC	PRPMOB	
ARORA	SRFMOB	
CONMOB	SRFMOB2	
PHUMOB	TFLDMOB	

In Medici there is a restriction on the total number of solution points which can be used in a simulation, the maximum is 10,000. These come in the form of a solution grid or mesh that is mapped over the user's device, which the user must design carefully to achieve good results. In section 4.3 I shall look at how the quantity and position of these points can effect the solution obtained.

As mentioned previously additional materials can be defined within Medici if required. Medici includes definitions for silicon, GaAs, polysilicon, aluminium gallium arsenide, indium gallium arsenide and silicon dioxide, among others. Changes to the physical properties of these materials such as permittivity, bandgap and density can be made to control the characteristics of a material. New materials can also be defined using the MATERIALS command.

4.3 Initial Investigations

In this section some of my initial investigations into GaAs MOSFET modelling are presented. This stage was necessary to gain proficiency in using Medici and to get some initial indications of what kind of results could be expected. The principles were then carried on throughout the drift-diffusion modelling part of the project, however the exact dimensions of devices and their design were not. Numerical device results are only included at this stage to illustrate the relative characteristic results

for silicon and GaAs devices.

An example silicon device structure was taken from the Medici manual to gain some insight into how to effectively use the Medici script-like description language. The device was kept as per the example with the only change being that the substrate was changed to GaAs, an InGaAs channel was added and the oxide was changed to Ga_2O_3. The resulting structure is shown in figure 4.1. In section 4.4 more physical doping values for GaAs will be discussed along with a fully calibrated model, as opposed to this simplified example.

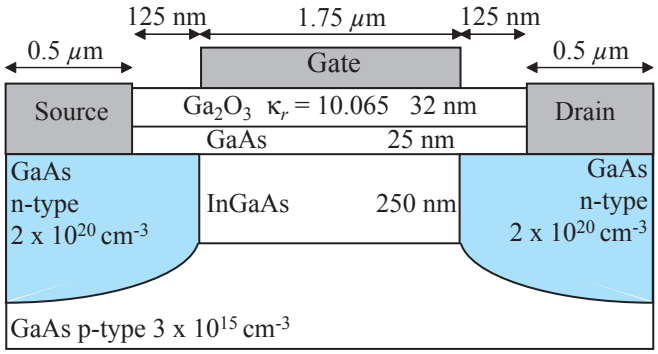
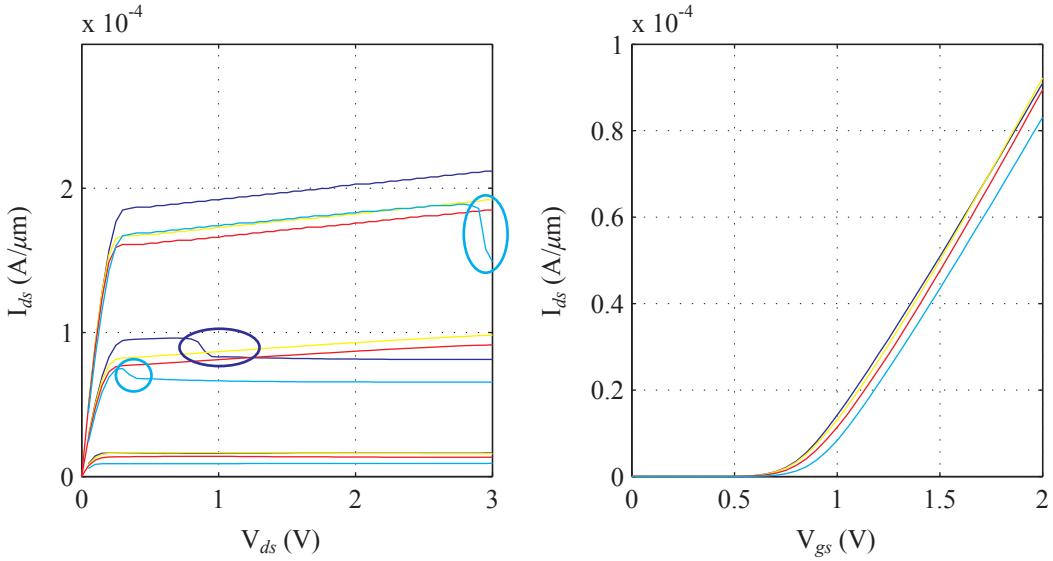


Figure 4.1: Structure of the initial GaAs NMOS device.

In figure 4.2 a comparison of the DC characteristics of the same device but with different mesh designs is shown. From this the importance of using a well designed mesh in device simulations is illustrated. As the mesh is refined the curves become smoother and give a more accurate representation of the devices characteristics. The circled areas on figure 4.2 illustrate errors due to poorly designed solution meshes. The most important factor is to have a high concentration of points located in and around the channel of the device, in the oxide and at the oxide-semiconductor interface of the device. The results of these investigations were essential in helping develop an efficient mesh design in section 4.4.

In figure 4.3 the result from figure 4.2(b) with the most refined mesh design (the curve in yellow) is graphed against the original silicon example. It can be seen that as expected the GaAs device has a considerably higher drive current than the silicon one. Additionally, it can be observed that the equivalent GaAs device has a larger threshold voltage.



(a) V_{gs} = 1, 1.5, 2 V (b) V_{ds} = 0.1 V

Figure 4.2: Drain and gate characteristics for the initial GaAs MOSFET structure. Each different colour represents the use of a different solution mesh.

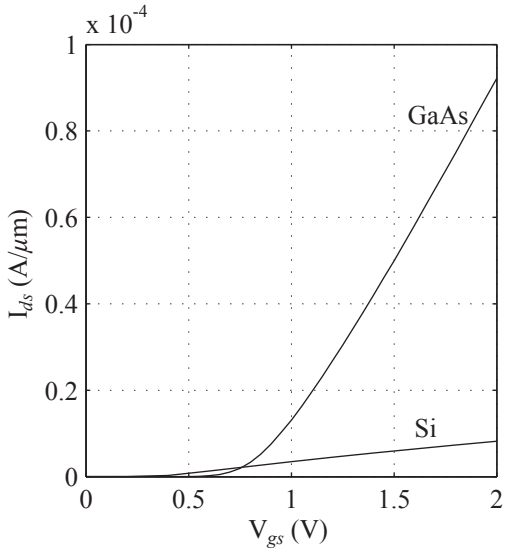


Figure 4.3: Comparison of GaAs and silicon gate characteristics at V_{ds} = 0.1 V.

4.4 Calibrating the GaAs PMOS Model

A key factor in developing the drift-diffusion MOSFET models was the decision to make models based on existing experimental device data wherever possible. This adds extra confidence in the models as they have been calibrated against real physical results rather than solely theory, as discussed in section 3.5.

When calibrating a device model, with respect to real physical data, there is key parameter information that aids the modellers confidence in their model. Firstly information on the device structure, this includes the gate length and width, the thickness of the different layers in the device, the position of contacts and the work function of the gate. Secondly information about the electro-active doping concentrations in the device are important. Finally, electrical measurements from the device are required. Ideally this would include measurements at different channel lengths and widths and bias conditions.

When choosing published data to base the devices on there were two key factors to consider. The first was which research was leading the field at the time. The second was the availability of data, as not all papers published give a full account of the characteristics of devices. My industry sponsor, Motorola, has led work in this field for many years and published many papers and registered patents in this area. Therefore Motorola/Freescale devices were a natural choice to base my models on.

Due to the limited amount of published data the size of devices investigated could not be in the deep sub-micron region. However, it is important to remember that the work presented is the first time that GaAs MOSFETs have been taken through these development stages and that this work shows a methodology which can be re-used in the future. Section 4.4.1 will detail the available device data and section 4.4.2 will detail how a PMOS heterostructure GaAs model was developed from this.

4.4.1 Available Information

In September 2002 Passlack *et al.* published data on a GaAs PMOS device [4]. This included some details of the device's structure and some electrical characteristic data. However, much of the necessary data for recreating the device to investigate it's performance was not published, in section 4.4.2 I shall discuss how this was dealt

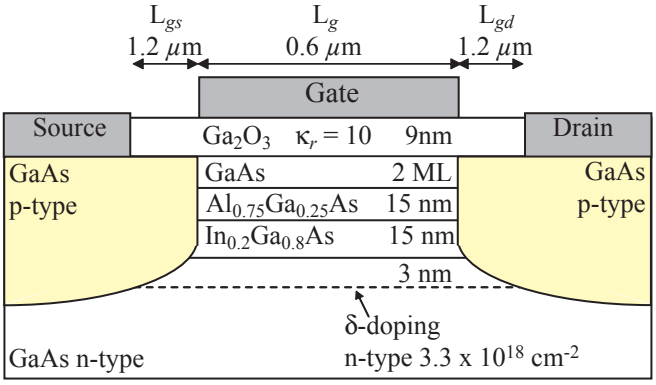


Figure 4.4: Structural information available for the GaAs PMOS device described by Passlack *et al.* [4].

with.

The data and simulation results shown in figure 3.4 and the structure shown in figure 3.5 were the starting point for the model development. Figure 4.4 shows all of the available structural data given in the published data, including the material properties that were given [4]. The gate oxide is a 9 nm thick layer of Ga_2O_3, which has a dielectric constant of 10. The GaAs layer directly underneath the oxide is two mono-layers thick and the $Al_{0.75}Ga_{0.25}As$ and $In_{0.2}Ga_{0.8}As$ layers are both 15 nm thick. The gate length of the device is 0.6 μm and the gate to source/drain spacing was $L_{gs} = L_{gd} = 1.2$ μm.

There is a δ-doping layer which is 3 nm below the InGaAs layer and has an areal density of 3.3×10^{11} cm^{-2}. The contact resistance is $R_c = 1.05$ Ωmm and implant sheet resistance is $\rho_S = 1234$ Ω/sq. The interface state density D_{it} is set to zero in the Motorola simulations. The measured maximum transconductance is $g_m = 51$ mS/mm and the simulated maximum transconductance $g_m = 77$ mS/mm. The measured threshold voltage is V_{th} = -0.93 V and the simulated threshold voltage V_{th} = -0.8 V. Device statistics for a 3" wafer were $g_m = 46.7 \pm 3.9$ mS/mm, V_{th} = -0.93 $\pm$ 0.1 V

4.4.2 Model Development

As discussed in section 4.4 there is certain key information that it is desirable to have for the development of a fully calibrated model. In section 4.4.1 it can be seen that

some of this information was available, such as the gate length, the layer structure of the device, the position of the contacts relative to one another and some electrical measurements from the device. This then leaves the gate width, work function of the gate and the doping concentrations of the substrate, source and drain to be investigated.

These unknown key parameters will be investigated in sections 4.4.2.1 to 4.4.2.5, where they will be optimised within known physical bounds and calibrated using the published gate and drain electrical characteristics for the device. Figure 4.5 shows a graphical representation of the work that follows in these sections. The model was constructed using Medici's script-like language and the final version of the code for the GaAs PMOS device is given in appendix B.

4.4.2.1 Defining Materials

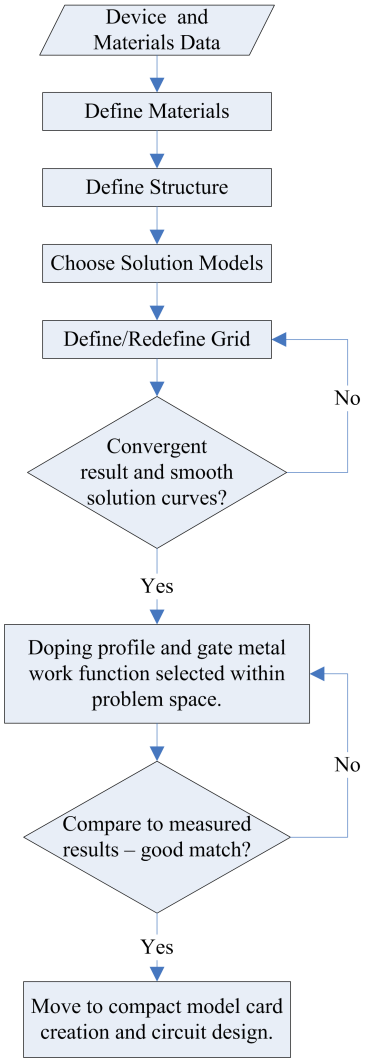
As mentioned previously Medici has many materials pre-defined, however Ga_2O_3 is not one of these. Therefore this must be manually defined by the user using the MATERIALS statement. Limited information was available on the properties of Ga_2O_3. The dielectric constant (PERMITTI) was known to be 10 (see section 4.4.1), the bandgap (EG300) is 4.9 eV [74], and the density (DENSITY) is 6×10^{-3} Kg/cm^3 [75]. The rest of the material properties were defaulted to the values for SiO_2. This was then defined in Medici as follows;

```
MATERIALS REGION=GA2O3 PERMITTI=10 EG300=4.9 DENSITY=0.006
```

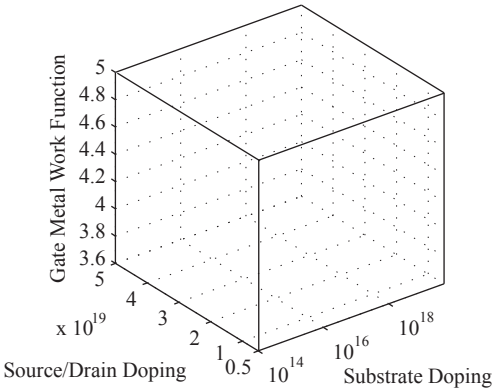
The dielectric constants of the other compound layers in the structure were also defined using the MATERIALS statement. This was to aid accuracy as in Medici the default properties for InGaAs and AlGaAs are the same as GaAs. The dielectric constants of the $Al_{0.75}Ga_{0.25}As$ and $In_{0.2}Ga_{0.8}As$ layers are 10.7 and 13.15 respectively [7].

4.4.2.2 Defining the Device Structure

Following from the data in section 4.4.1 it was necessary to define some additional parts of the device structure illustrated in figure 4.4.



(a) This is a detailed account of how Stage 5 of the new device-to-market design flow (figure 3.8) was completed in this project.



(b) Problem Space.

Figure 4.5: Modelling development stages and unknown parameter problem space.

The thickness of two mono-layers of GaAs must be defined, which is approx 0.5 nm as shown in the literature [76, 77]. The thickness of the δ-doping layer was chosen to be 1 nm, and the depth of the device structure was 2 μm from the bottom of the oxide to the bottom of the substrate.

The length of the source and drain contacts had to be chosen and were assumed to be 0.5 μm, which is is a reasonable value for a device of this size. This value is fairly arbitrary as the source and drain to gate distances were known and the contact and sheet resistances were known. Medici requires the resistances in $\Omega\mu m$ which makes the contact resistance R_c = 1050 $\Omega\mu$m and the implant sheet resistance ρ_S = 1480.8 $\Omega\mu$m. To add these into the Medici model they were added together as a lumped resistances on both the source and drain contacts using the following commands.

```
CONTACT NAME=Source RESISTAN=2530.8
CONTACT NAME=Drain RESISTAN=2530.8
```

Finally, the width of the device was not explicitly given, however it was possible to calculate this from the electrical characteristics that were given. The gate and drain characteristic data were extracted from the paper using *datathief*. *Datathief* is a piece of software that allows the user to extract data from a graphic by superimposing axes with maximum and minimum bounds. The gate characteristics were in mA/mm and translated into A/μm and drain characteristics which were in mA were translated into A. Figure 4.6 illustrates the measured gate characteristics in blue and a series of data points taken from the drain characteristics in green. To achieve the matching of these curves the drain data had to be divided by 10, implying a gate width of 10 μm.

Figure 4.7 shows the characteristic data from the paper in A/μm assuming a width of 10 μm. It also shows two additional curves for the gate characteristics at V_{ds} = -0.5 V and -2.5 V which were extracted from the drain characteristics. It is important to calibrate the device characteristics at both high and low drain biases. V_{ds} = -0.5 V was the lowest distinguishable gate characteristic that could be extracted from points on the published drain characteristics. V_{ds} = -2.5 V was the highest value given in the drain characteristics

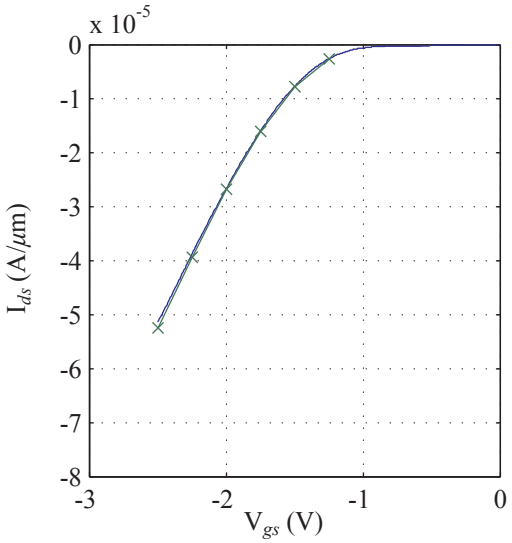
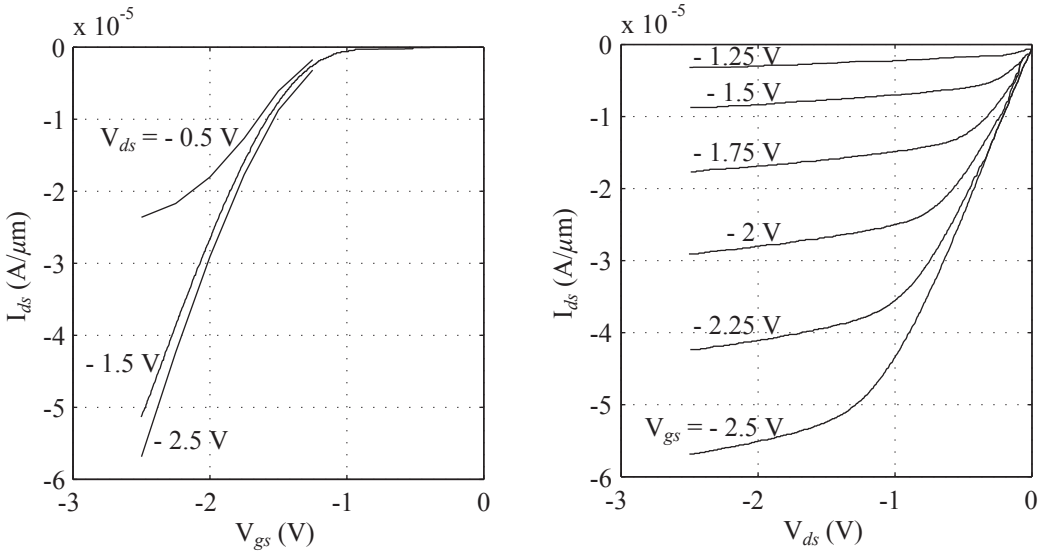


Figure 4.6: GaAs PMOS gate characteristics at V_{ds} = -1.5 V from Passlack *et al.* [4]. The blue curve is as the measured results in figure 3.4(a), the green curve is extracted from data in figure 3.4(b).



(a) Gate characteristics.

(b) Drain characteristics.

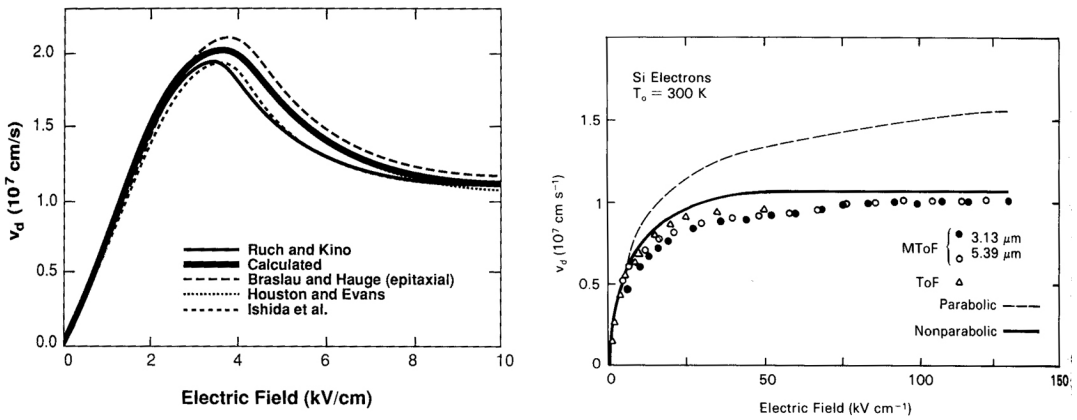
Figure 4.7: GaAs PMOS gate and drain characteristics from [4] used for PMOS device calibration.

4.4.2.3 Solution Models

In addition to the default solution methods in Medici to achieve a more accurate result and to improve the convergence of models is advantageous to introduce additional solution methods. There are three of the Medici mobility models that specifically have an option for solving GaAs-like materials; CONMOB, ANALYTIC and FLDMOB. As shown in table 4.1

CONMOB is a concentration dependent mobility model which uses look up tables to relate the doping concentration to a mobility value. ANALYTIC is an alternative to this which is both concentration and temperature dependent. These models are mutually exclusive, so ANALYTIC was chosen.

If FLDMOB=2 is selected, as the electric field increases the carrier drift velocity reaches a peak and then begins to decrease at high fields due to the transferred electron effect, this gives a more GaAs like mobility behaviour. To illustrate how the material properties differ, Figure 4.8(a) shows the typical velocity versus electric field curve for GaAs and Figure 4.8(b) shows the equivalent curve for silicon.



(a) GaAs (b) Si

Figure 4.8: Measured and calculated drift velocity versus electric field at 300 K [7].

To take account of transverse field effects PRPMOB was also chosen. I found that during the various iterations of PMOS device calibration that the inclusion of these mobility models aided the convergence of simulations.

A one carrier Newton solution was used to simulate the devices. However the solution for a bias point did not always converge on a result within the default of

four iterations. To improve convergence of the simulations the maximum number of iterations was increased from the default to ten.

4.4.2.4 Solution Grid Design

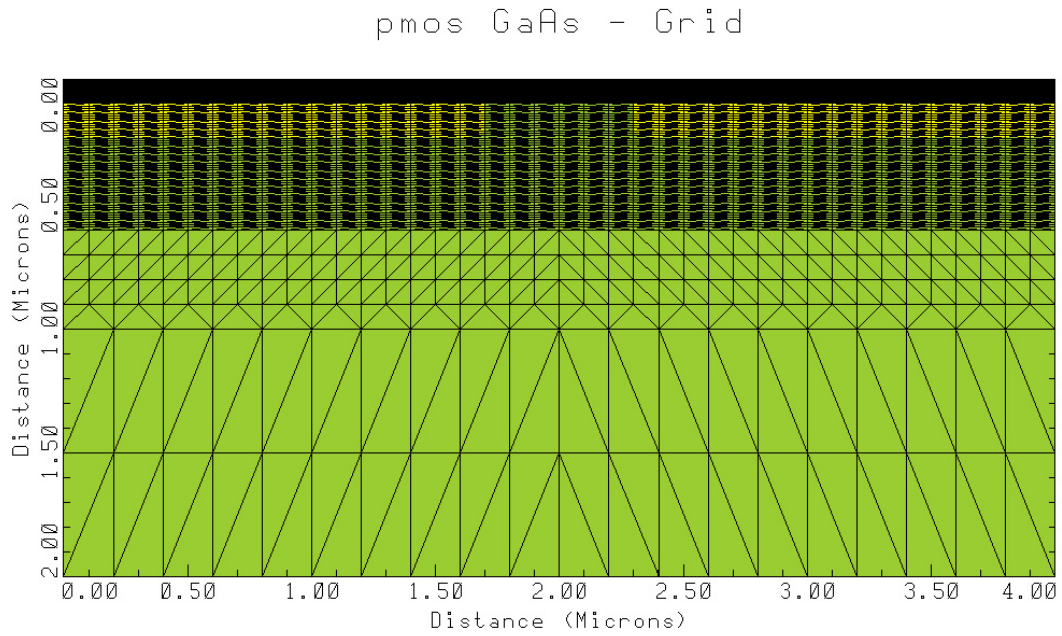
The solution grid was designed based on the results found in section 4.3. The Medici code to describe this is shown in appendix B. Figure 4.9 illustrates the grid design used.

The grid spacing from left to right is every 100 nm. The grid spacing from the top to the bottom of the device varies depending on the layer of the device as shown in figure 4.10. As discussed previously it is critical to carefully choose the design of the solution grid as the maximum number of points is constrained. In most cases a simple uniform grid using even the maximum number of points over a device would provide insufficient granularity for the key areas of the device, such as the oxide-semiconductor interface and the channel of the device. As shown in figure 4.10 the grid spacing has been made much smaller in these critical areas, the minimum grid spacing used is 0.1 nm.

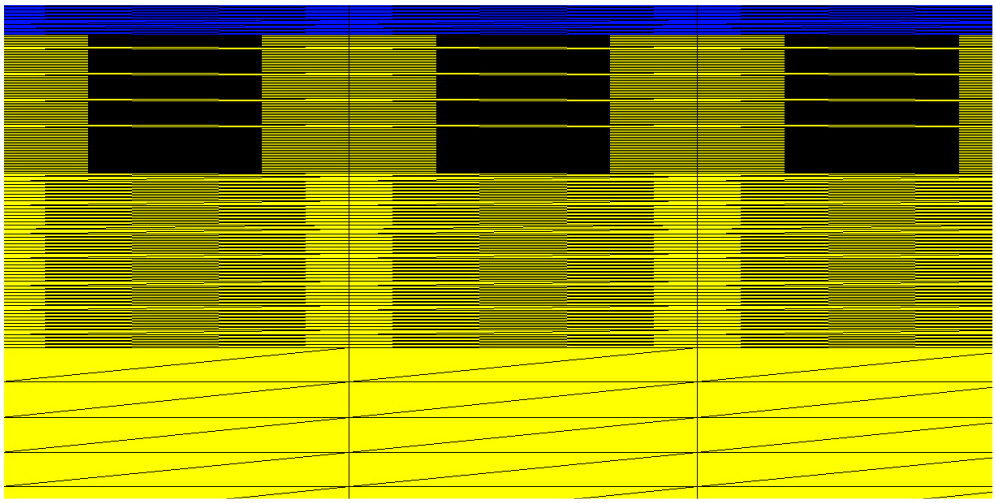
4.4.2.5 Doping and Gate Work Function

As mentioned previously the device doping concentrations and gate work function were unknown and had to be investigated. This was done via Medici simulations and by considering the MOSFET equations for the current in the linear region (equation 4.6a) and the saturation region (equation 4.6b) of device operation.

In equations 4.6a and 4.6b, μ_{eff} is the effective mobility. The selection of the correct mobility models in Medici should ensure that the mobility is this is correct in the GaAs device (see section 4.4.2.3). C_{ox}, is the oxide capacitance. Medici calculates the capacitances within the device depending on the structure that is specified (it will be shown in section 4.4.3 that by correct device design the channel was formed in the InGaAs layer as required). W and L, the width and length of the device, are known as discussed in sections 4.4.1 and 4.4.2.2. The correct channel length is achieved by careful design of the source and drain which will be discussed presently. V_{gs} and V_{ds} are gate-to-source and drain-to-source biases for the device, these are set as in the characteristics shown in figure 4.7. V_{th} is the

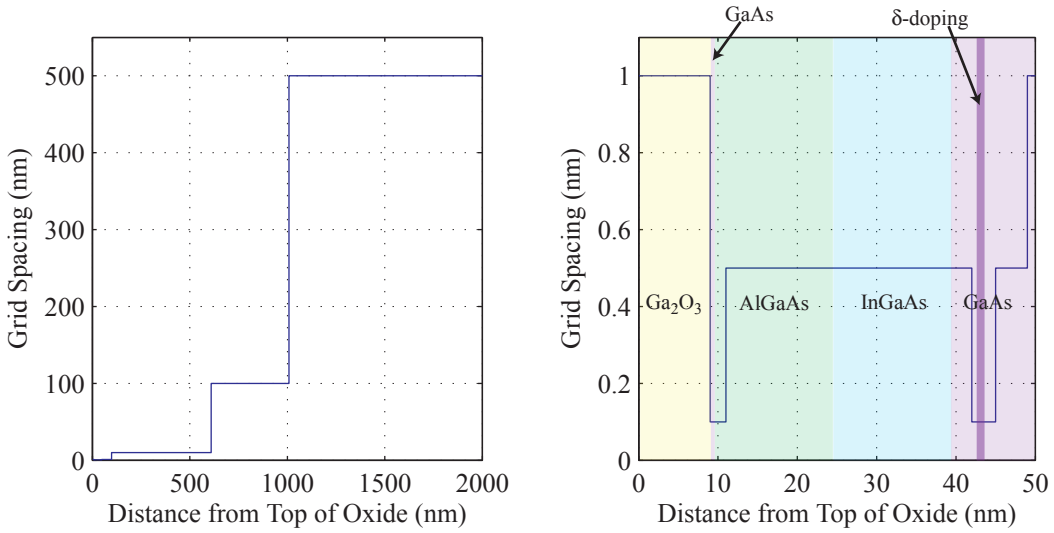


(a) Full grid.



(b) Top left detail.

Figure 4.9: Solution grid for the GaAs PMOS device.



(a) Whole device. (b) Detail.

Figure 4.10: Vertical grid spacing in devices.

threshold voltage of the device, the equations for calculating this are shown in 4.7. The threshold voltage of the Motorola device was known to be -0.93 V.

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L}(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2 \tag{4.6a}$$

$$I_{sat} = \mu_{eff} C_{ox} \frac{W}{2L}(V_{gs} - V_{th})^2 \tag{4.6b}$$

$$V_{th} = -\frac{Q_{dm}}{C_{ox}} + 2\psi_B - V_{fb} \tag{4.7a}$$

$$Q_{dm} = -qN_s X_j \tag{4.7b}$$

$$\psi_B = \frac{k_B T}{q} ln\left(\frac{N_s}{n_i}\right) \tag{4.7c}$$

$$X_j = \sqrt{\frac{4\epsilon_s \psi_B}{qN_s}} \tag{4.7d}$$

$$V_{fb} = \phi_m - \phi s \tag{4.7e}$$

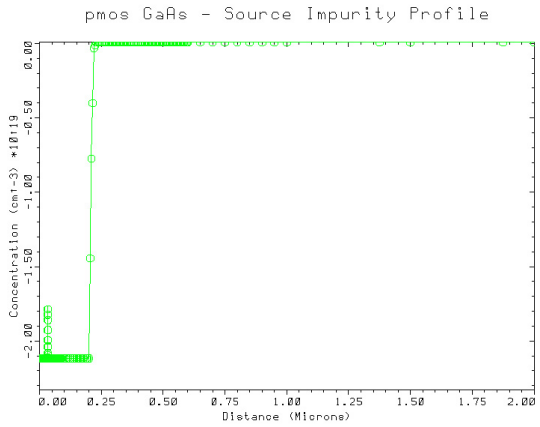
To obtain the correct threshold voltage (V_{th}) for the device the correct choice of substrate doping (N_s) and work function for the gate metal (ϕ_m) is vital, as can be seen from equation 4.7. Where Q_{dm} is charge in the depletion layer, ψ_B is Fermi potential in the substrate (or bulk), X_j is the width of the depletion layer or junction depth, n_i is the intrinsic carrier concentration of the substrate, V_{fb} is the flat band voltage and ϕ_s is the work function of the substrate. The other parameters are as described previously.

As can be seen in equation 4.7c the substrate doping has to be greater than the intrinsic carrier concentration for a physically correct solution, n_i for GaAs is 2.1×10^6 cm^{-3} [7]. The literature indicates that the substrate doping for a semi-insulating GaAs substrate should be of the order of 10^{16} cm^{-3} [34]. A substrate n-type doping of 8×10^{16} cm^{-3} was found to give the best fit to the data.

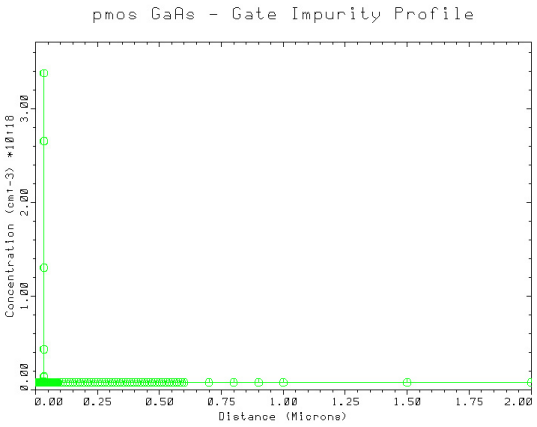
The shape of the source and drain doping profiles was kept simple as no information was available about this, and as the gate length of the device is relatively long, i.e. not deep sub-micron, the only important issue for the shape of the source and drain is that it creates the correct channel length. Additionally, it is important to consider that in the next chapter where compact models are created, only the doping value and the channel length are used and no complex information about doping profiles can be included.

The source and drain regions are required to be highly doped and less than the maximum possible doping, which is 5×10^{19} cm^{-3} for GaAs [64]. The source and drain are p-type and a doping of 2.125×10^{19} cm^{-3} was found to give the best fit and is physically realistic for such a device. Figure 4.11 illustrates the doping profiles.

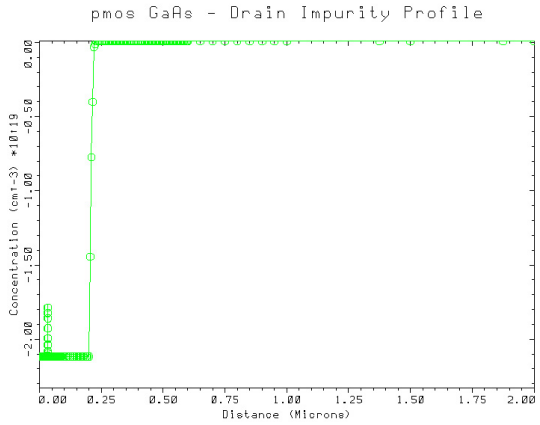
When investigating the gate metal work function, 4.55 eV was used as a starting point as this was what was used in the Motorola simulations [4]. However, as their simulation results were significantly different to their device results and in fact the threshold voltage that they observed in their simulations was -0.8 V this was altered along with the substrate doping to achieve a threshold voltage closer to the measured results. It was found that a work function of 4.68 eV gave the best fit to the measured data. This falls within realistic bounds for the gate metal compound titanium tungsten nitride (TiWN) which was used in the fabricated device [78].



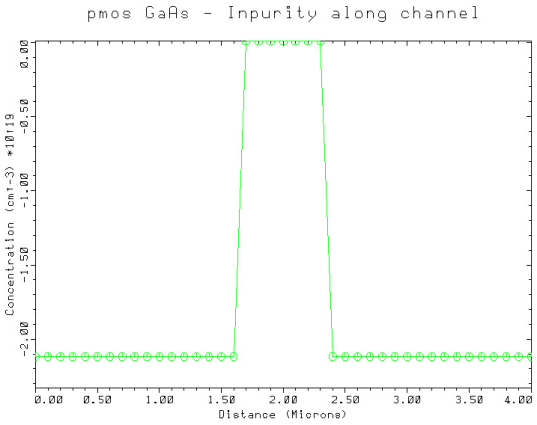
(a) Doping profile of the source.



(b) Doping profile under the gate, the spike shows the position of the δ-doping.



(c) Doping profile of the drain.



(d) Doping along the channel of the device, which shows the position of the source and drain doping.

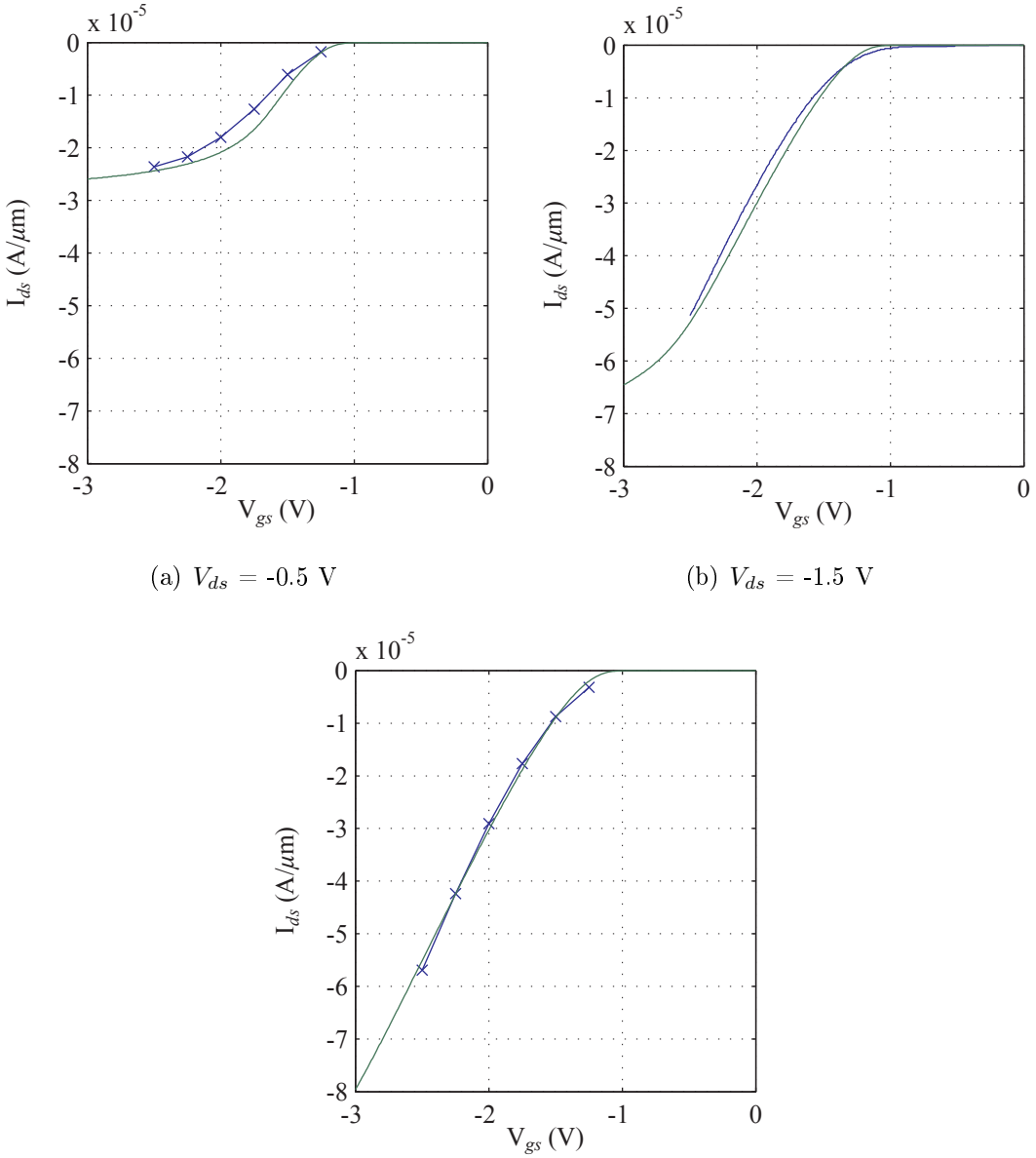
Figure 4.11: (a), (b) and (c) show doping profiles down through the PMOS device. Where zero is at the oxide-semiconductor interface. (d) shows doping along the device from left to right.

4.4.3 Results and Discussion

As discussed throughout this chapter it is critically important for device models to be calibrated thoroughly against measured device data. MOSFET data was selected based on the availability of measured data, and the interests and research activities of my company sponsor. As only PMOS device data was available this was used as a starting point to develop a calibrated GaAs/Ga_2O_3 physical model. In the next section it will be shown how, from the PMOS model development, a complimentary NMOS device was also modelled. This was necessary to fully investigate the circuit design issues with GaAs, which will be addressed in chapter 6.

The resulting gate and drain characteristics for the PMOS Medici drift-diffusion model are shown in figure 4.12 and figure 4.13(a) respectively, along with the measured data. It can be seen that a good agreement is achieved. The drain characteristics for the GaAs PMOS model are also compared to the drain characteristics of a silicon device of the same size in figure 4.13(b) (details of the silicon models used are given in appendix C). As expected, the drive current in a similarly-sized silicon PMOS device is better than the GaAs device due to the slightly higher hole mobility.

Simulations show that when the device is on the channel is formed near the top of the InGaAs layer. This can be seen in figure 4.14, where the majority charge carriers, holes in the case of a PMOS device, can be observed as grouping in this region. To further illustrate physically correct device operation, the charge carrier positions are illustrated in three key regions; when the device is off, sub-threshold, and on. Figure 4.15 shows how the charge carriers change position as the device transitions from off (figures 4.15(a) and 4.15(b)) through sub-threshold (figures 4.15(c) and 4.15(d)) to on (figures 4.15(e) and 4.15(f)). When the device is off the majority charge carriers (holes) are present in the InGaAs channel but at a much lower concentration than the inhibiting electrons. This is illustrated in figures 4.15(a) and 4.15(b). As the voltage is increased (figures 4.15(c) and 4.15(d)) the hole concentration increases but not yet beyond that of the electrons. Once the gate voltage is increased above the threshold voltage the majority of the electrons are pushed down beneath the channel, and the hole concentration finally supercedes that of the electrons, and MOSFET is on.



(a) V_{ds} = -0.5 V

(b) V_{ds} = -1.5 V

(c) V_{ds} = -2.5 V

Figure 4.12: GaAs PMOS gate characteristics. Medici drift-diffusion results (green) compared to the Motorola measured results (blue).

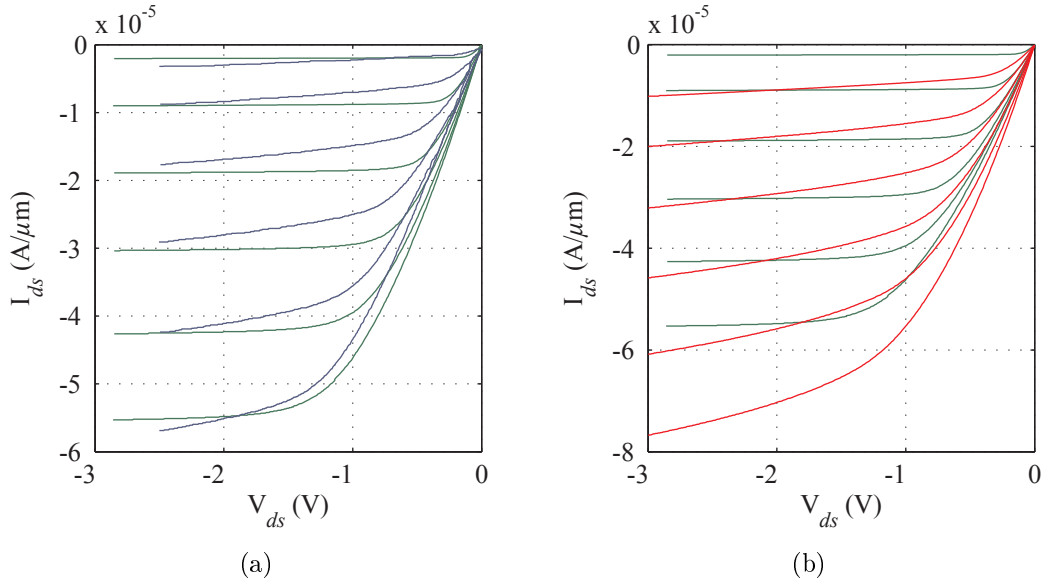


Figure 4.13: GaAs PMOS drain characteristics, where -2.5 V $\leq V_{gs} \leq$ -1.25 V at 250 mV intervals for each family of curves. In (a) Medici drift-diffusion results (green) are compared to the Motorola measured results (blue). In (b) Medici drift-diffusion results (green) are compared to a similarly-sized silicon device (red).

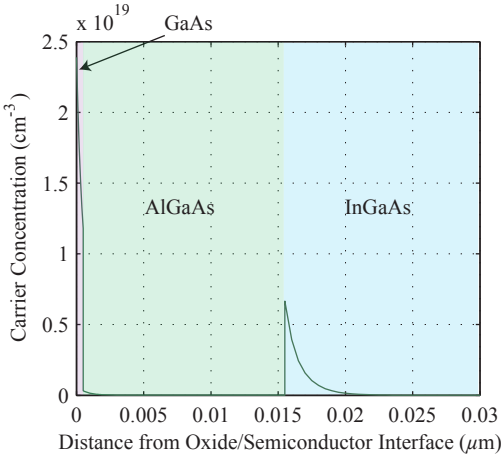
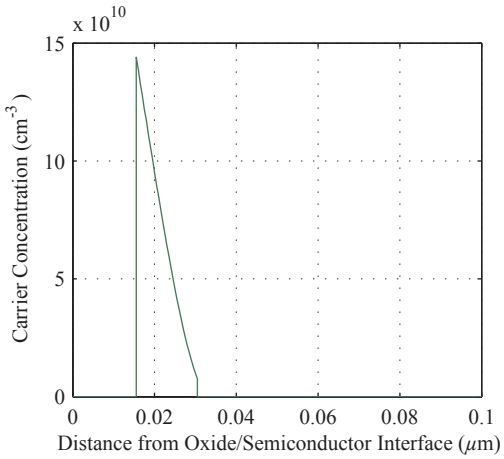
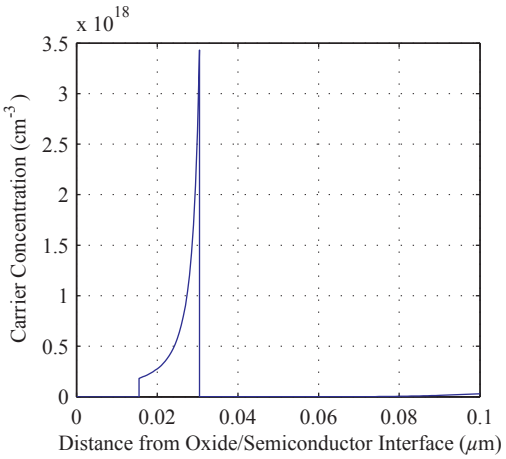


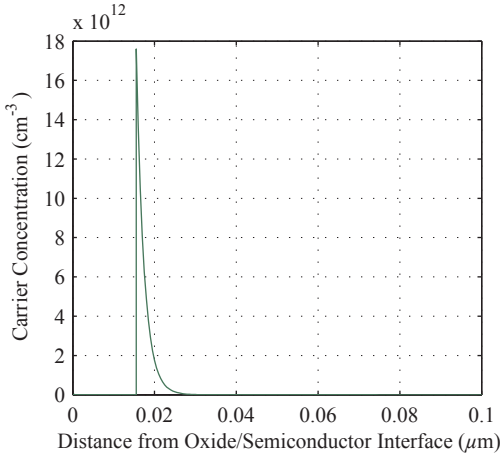
Figure 4.14: Majority carrier concentration (holes) in the GaAs PMOS device when the device is on. V_{gs} = -1.5 V, V_{ds} = -1.5 V.



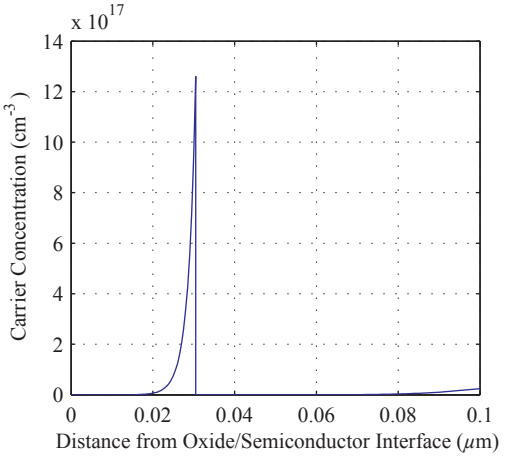
(a) Holes, V_{gs} = 0 V, V_{ds} = 0 V



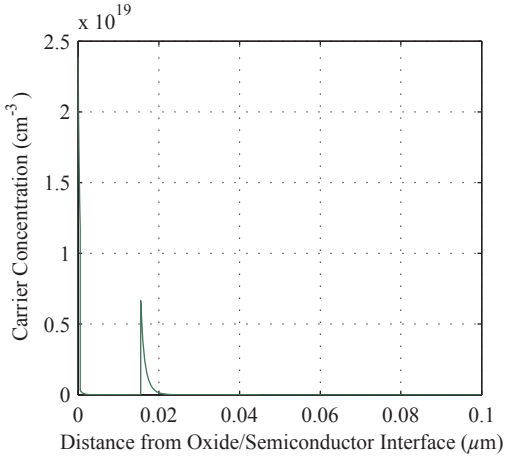
(b) Electrons, V_{gs} = 0 V, V_{ds} = 0 V



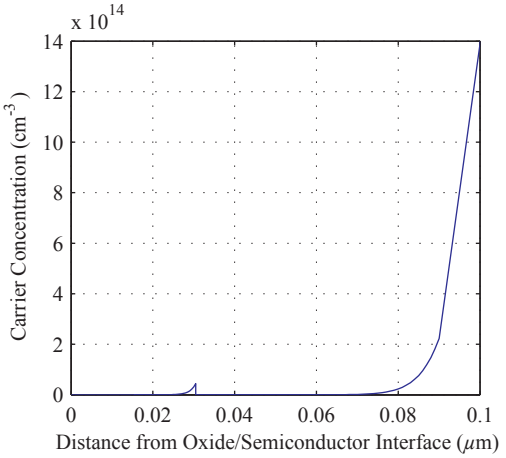
(c) Holes, V_{gs} = -0.5 V, V_{ds} = -1.5 V



(d) Electrons, V_{gs} = -0.5 V, V_{ds} = -1.5 V



(e) Holes, V_{gs} = -1.5 V, V_{ds} = -1.5 V



(f) Electrons, V_{gs} = -1.5 V, V_{ds} = -1.5 V

Figure 4.15: Carrier concentrations in GaAs PMOS device when the device is (a)(b) off, (c)(d) sub-threshold, and (e)(f) on.

Simulations also show that the mobility of the holes in the channel of the PMOS device is 240 cm^2/Vs, which is in good agreement with the literature [79]. This is shown in figure 4.16.

All of these results indicate that the PMOS device behaves in a physically correct manner, and that it's electrical characteristics match those of the measured device characteristics being used for the calibration. The next stage is to create a complimentary NMOS GaAs device from the knowledge gained from the PMOS investigation.

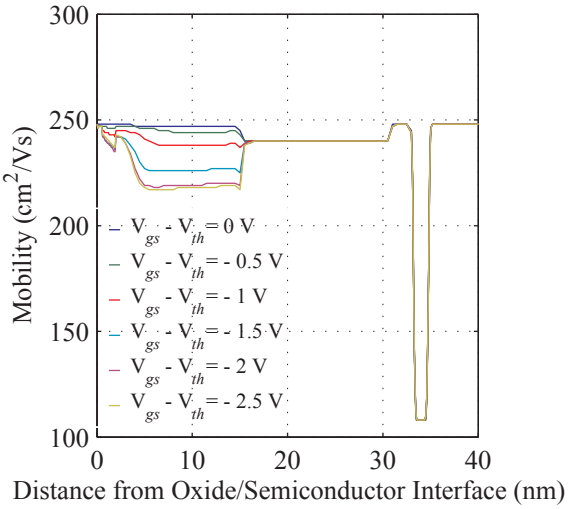


Figure 4.16: Mobility of holes in the GaAs PMOS device down through it's centre. V_{ds} = -1.5 V

4.5 CMOS from PMOS

In order to investigate the anticipated properties of a CMOS technology, a complementary GaAs NMOS device model is constructed. In the absence of measured device data for GaAs NMOS devices, drift-diffusion simulations are used to build a structure complementary to the PMOS device to obtain an indication of potential performance. It is assumed that the device structure is the same the PMOS device with the exception of doping, where p-type regions become n-type and vice versa. As discussed earlier Medici's solution models will ensure that based on this structure,

where the electrons will now be the majority charge carriers, the device's physical properties will be calculated correctly. The Medici code for the device is shown in appendix D.

The drain characteristics for the GaAs NMOS are illustrated in figure 4.17 along with results for a similarly-sized silicon device. It can be seen that once the gate voltage is set to ≥ 1.5 V, the GaAs NMOS device has a significantly higher drive current than the silicon equivalent. The electron mobility in the InGaAs channel of the NMOS device is estimated to be 1500 cm^2/Vs from simulation results (figure 4.18).

As GaAs NMOS devices are explored and optimised in the future through fabrication and modelling, improvements may be observed in the mobility and drive current. There are several ways in which improvements might be seen such as lowering the contact resistant in devices and decreasing the gate length. Also improvements in how the heterostructure is constructed, such as the thicknesses and positions of the layers used, and the mole fractions of the chemicals in the ternary compounds that are used may improve the characteristics.

4.6 Summary

In this chapter physical device models of GaAs MOSFET devices were developed based on measured device data. This was done using a drift-diffusion based device simulator, and the underlying theory has been discussed with reference to the tools being used. The physics of the devices were carefully considered as part of the calibration process, with issues such as the physical maximum doping concentrations and the material properties of the heterostructure layers and gate metal being significant.

These types of heterostructure devices are more challenging to simulate than traditional silicon devices, as the onus is on the designer to have an understanding of the material properties. This is due to the fact that in the simulator (Medici) the material properties for the required ternary compounds are defaulted to those of GaAs and the dielectric material (Ga_2O_3) is not included in the materials database.

Convergence issues were solved by careful solution grid design and choosing appropriate solution models. The device characteristics were calibrated by building a model based on the known device layer structure and by choosing appropriate

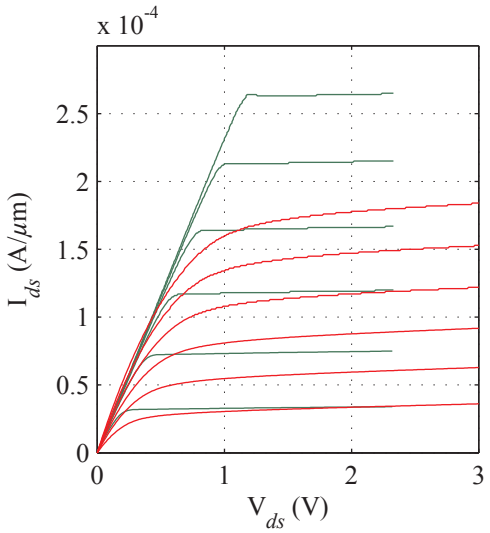


Figure 4.17: GaAs NMOS drain characteristics. Medici drift-diffusion results (green) compared to a similarly-sized silicon device (red). Where 1.25 V $\leq V_{gs} \leq$ 2.5 V at 250 mV intervals for each family of curves.

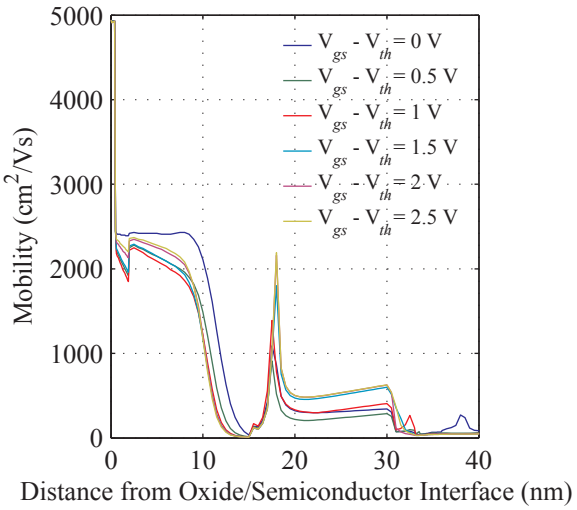


Figure 4.18: Mobility of electrons in the GaAs NMOS device down through it's centre. V_{ds} = 1.5 V

doping profiles and gate work function. The resulting device characteristics show that the PMOS drift-diffusion models are calibrated to the data. From the PMOS results, a complimentary NMOS device has also been modelled. This was necessary to enable the circuit design investigation which follows in chapter 6.

There is another necessary stage before these drift-diffusion models can be used in a circuit design environment; they must be translated into compact models. In the next chapter these compact models will be developed.

5 Compact Model Development

5.1 Introduction

Following on from the work presented in chapter 4, in this chapter I will discuss the development of compact models based on the drift-diffusion Medici results. These can then be used with a SPICE simulator to investigate circuit design for GaAs MOSFETs. The Berkeley BSIM3 compact model, version 3.2, was used as this was the most up to date version at the time of development.[1] Cadence integrated circuit design tools, which include the SPICE simulator Spectre, were used to generate the simulation results.

[1] BSIM3v3.3 has since been released, which has improved noise models. BSIM4 is also now available for use with devices in the sub-100 nm regime.

Compact models are by their nature an approximation to true device physics, allowing circuit simulations to be run on a more acceptable time scale. They are used extensively in industry and give an excellent simulation result. The key with developing compact models, as with any model, is to achieve a good calibration with the data. It will be shown how this was achieved.

Compact models do not allow the same degree of freedom as the drift-diffusion modelling tools discussed previously. As a consequence, there is less transparency and control over the model. This proved to be the key issue in developing the compact models, specifically for GaAs MOSFETs. Every effort was made to develop compact models that reflected, wherever possible, the realities of the device physics and materials data for the GaAs devices.

5.2 An Introduction to the BSIM Compact Model

Berkeley BSIM is a physics-based, industry standard, compact MOSFET SPICE model for circuit simulation and CMOS technology development. It has been developed by the BSIM Research Group at the University of California, Berkeley. The third version of this (BSIM3v3) was established by SEMATECH as the first industry-wide standard of its kind in December of 1996. BSIM3v3 has since been widely used by most semiconductor and integrated circuit design companies worldwide for compact device modelling and CMOS IC design.

BSIM3v3.2 has 150 parameters which can be used to customise it's Si/SiO_2 compact SPICE model. Using these parameters it is possible to control a device's current (I-V) and capacitance (C-V) characteristics, it's temperature dependence, and some of the process related parameters. Details of these parameters and the equations that comprise the BSIM model are described in section 5.4, where they are used to develop an adapted GaAs model.

5.3 Adapting BSIM for $GaAs/Ga_2O_3$ Devices

Creating a BSIM model for a silicon device is usually done using an automated parameter extraction strategy. One technique uses the parameter extraction tool Aurora in conjunction with results generated by Medici. This involves translating

the files from the Medici format, importing them into Aurora, developing an extraction strategy, and then completing the parameter extraction. Although this method was investigated for this project, it was decided that it would be inappropriate for two main reasons.

The first is that to develop a good extraction strategy many different devices of varying gate lengths and widths, of the same internal structure, are required. To provide data from Medici on devices with different gate lengths requires either, measured results from different sized devices for calibration, or the theoretical scaling of devices. The principle was to develop models based on real device data, therefore theoretical device scaling did not fit with the methodology. Additionally, as discussed previously, information about different device characteristics was limited.

Secondly, using an automated extraction strategy would never accurately model the physics of a GaAs device. Hence, to achieve compact models that could be considered to be as physically accurate as possible, a more tailor-made approach was used.

The BSIM model was developed for use with Si/SiO_2 devices, therefore in adopting the BSIM model for GaAs, it is assumed that the GaAs MOSFET behaves in a physically similar way to a silicon MOSFET. There are three fundamental physical constants that are inaccessible in the BSIM3v3.2 model that are fixed as the values for Si/SiO_2; the permittivity of the semiconductor (ϵ_s), the intrinsic carrier concentration of the semiconductor (n_i) and the permittivity of the oxide (ϵ_{ox}). In order to use the BSIM3v3.2 model for the proposed $GaAs/Ga_2O_3$ MOSFET models, it was necessary to compensate for these physical properties.

In almost all cases n_i and ϵ_{ox} appear in the following ratios in the BSIM model equations: N_{ch}/n_i; N_s/n_i and ϵ_{ox}/t_{ox}, where N_{ch} is the channel doping concentration, N_s is the substrate doping concentration, and t_{ox} is the thickness of the oxide. Since N_{ch}, N_s, and t_{ox} can be accessed by the user, the ratios can be corrected for $GaAs/Ga_2O_3$. Exceptions where these parameters are found outside the ratios will be discussed in section 5.4. As the permittivity of GaAs ($\kappa_{GaAs} = 13.1$) is very close to that of silicon ($\kappa_{Si} = 11.9$) is not corrected for. However, the GaAs value is used in all manual calculations made.

In order to build a full BSIM model card, process parameters are either taken directly from the drift-diffusion model values or calculated using the BSIM equa-

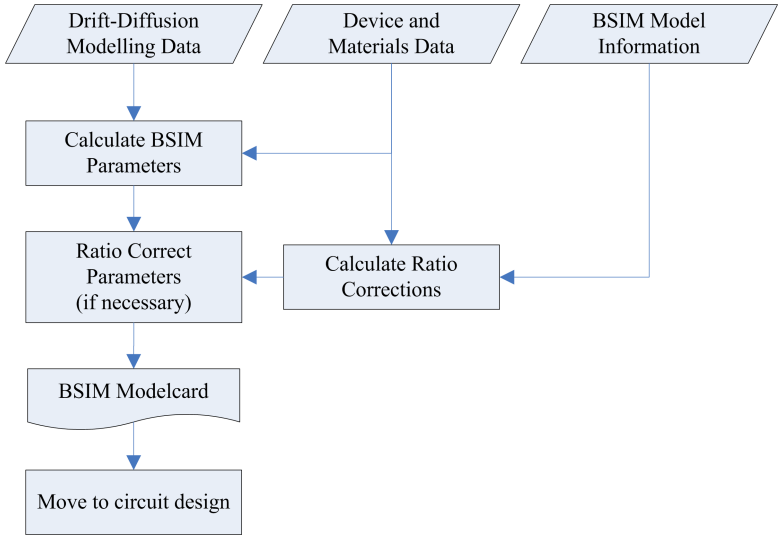


Figure 5.1: This is a detailed account of how Stage 6 of the new device-to-market design flow (figure 3.8) was completed in this project.

tions. The majority of the DC and C-V parameters are established in a similar manner, with some default values being used where this is not possible. The non-quasi static model parameters, length and width offset parameters, temperature parameters, flicker noise model parameters, and geometry range parameters are set to the BSIM3v3.2 default values. Appendix E details the default BSIM parameters [80]. All of the BSIM calculations that are made use the GaAs/Ga_2O_3 physical properties. The doping values (N_{ch} and N_s) and oxide thickness (t_{ox}) are then adjusted to ensure that the aforementioned ratios are correct. In addition, some BSIM numerical factors are compensated to ensure that calculations made internally by the model are correct for GaAs/Ga_2O_3. This is mainly due to the fact that there are some instances where N_{ch}, N_s, n_i, ϵ_{ox} and t_{ox} do not appear in the ratios discussed. However these are in the minority and can be addressed by adjusting some additional parameters. Figure 5.1 illustrates the development stages. The BSIM values and calculations are detailed in section 5.4. The calculations are all specifically for the GaAs devices previously described. However, the methodology presented of using ratio corrections to adapt BSIM models for use with unconventional devices stands, and is generally applicable and adaptable to future devices, both GaAs and otherwise.

5.4 BSIM Parameter Calculations and Definitions

In this section the BSIM model parameters will be presented along with the relevant calculations. Appendix F shows the resulting model card in the Cadence Spectre format, which can be translated for use with other SPICE simulators if required. This compact model file is used in chapter 6 to assess potential circuit performance.

As the NMOS and PMOS devices have the same structure and doping quantities and many of the parameter values are the same for them both. Where they are different this will be indicated and both calculations shown. In addition to the parameters listed there are some extra definitions required for the Cadence Spectre model cards. As shown in appendix F just before a device's parameter list there are two extra definitions. The first is the inclusion of *bsim3v3*, this specifically tells the simulator the type of compact model being used (there are many predecessors to BSIM3v3.2). The second is the *type* parameter, this is set to either p or n for PMOS and NMOS devices respectively.

5.4.1 Process Parameters

It is here in the process parameters that the ratio corrections discussed previously are essential. The process parameter values are used in many of the internal BSIM equations to calculate other values so it is essential that they are correct. Table 5.1 shows both the physical calculated GaAs values and the ratio corrected values (where applicable), the method and calculations for these follow.

As discussed in chapter 4 the channel of the device is formed at the top of the InGaAs layer. Therefore the oxide can be considered as effectively being composed of the three layers above this (Ga_2O_3/GaAs/AlGaAs). Using a form of effective medium theory, is is possible to find a single effective dielectric constant (κ_{eff}) for this effective oxide [81]. To do this we consider the heterostructure layers above where the channel is found, as shown in figure 5.2. Using equation 5.1 it can be shown that the resulting dielectric constant is 10.49. Where, κ_i, t_i, and d_i are the dielectric constant, thickness, and partial thickness of a particular layer, respectively. T is the total thickness of all of the layers, and n is the number of layers. Therefore t_{ox} = 24.5 nm and κ_{oxGaAs} are the effective values for the GaAs device. These values are used in all manual calculations for the BSIM parameters.

Table 5.1: BSIM3v3.2 Process Parameter Values

Symbol Used in Equations	Symbol Used in SPICE	GaAs Value	Ratio Corrected Value
t_{ox}	tox	24.5×10^{-9} m	9×10^{-9} m
X_j	xj	1.512×10^{-7} m	no RC
N_{ch}	nch	8×10^{16} cm^{-3}	5.57×10^{20} cm^{-3}
N_s	nsub	8×10^{16} cm^{-3}	5.57×10^{20} cm^{-3}
γ_1	gamma1	0.454 V$^{1/2}$	no RC
γ_2	gamma2	0.454 V$^{1/2}$	no RC
X_t	xt	19×10^{-9} m	no RC
V_{bx}	vbx	1.24 V	no RC

Ga_2O_3	$\kappa_{Ga_2O_3} = \kappa_1 = 10$	$t_1 = 9$nm
GaAs	$\kappa_{GaAs} = \kappa_2 = 13.1$	$t_2 = 0.5$nm
$Al_{0.75}Ga_{0.25}As$	$\kappa_{Al_{0.75}Ga_{0.25}As} = \kappa_3 = 10.7$	$t_3 = 15$nm

Figure 5.2: Dielectric constants in the effective oxide of the heterostructure.

$$\begin{aligned} d_i &= \frac{t_i}{T} & \kappa_{eff} &= \sum_{i=1}^{n} \kappa_i d_i \\ T &= \sum_{i=1}^{n} t_i & &= 10.49 = \kappa_{oxGaAs} \\ &= 24.5nm = t_{ox} \end{aligned} \tag{5.1}$$

These parameters are particularly essential for calculating the oxide capacitance, C_{ox} (see equation 5.2). Where ϵ_{ox} is the permittivity of the oxide, κ_{ox} is the dielectric constant of the oxide, ϵ_0 is the permittivity constant, and t_{ox} is the oxide thickness. The correct value for the GaAs devices is shown in equation 5.3. However, BSIM assumes the dielectric constant of the oxide to be that of silicon dioxide. Therefore, if these values are used without any ratio correction, BSIM returns the incorrect value for C_{ox} as shown in equation 5.4. Thus, if the GaAs device value for t_{ox} is used in the BSIM model card without any adjustment, the oxide capacitance would be out by a factor of ≈ 2.5. This can be resolved as shown in equation 5.5, where

t_{ox} is the effective GaAs device value for the oxide thickness (24.5 nm), and t_{ox}^{RC} is introduced as the *ratio corrected* oxide thickness. t_{ox}^{RC} is the value that will be used in the BSIM model card.

$$\begin{aligned} C_{ox} &= \frac{\epsilon_{ox}}{t_{ox}} \\ &= \frac{\kappa_{ox}\epsilon_0}{t_{ox}} \end{aligned} \tag{5.2}$$

$$\begin{aligned} \kappa_{ox} &= \kappa_{oxGaAs} = 10.49 \\ C_{ox} &= \frac{\kappa_{ox}\epsilon_0}{t_{ox}} \\ &= 3.79 \times 10^{-3}\ \mathrm{F/m^2} \end{aligned} \tag{5.3}$$

$$\begin{aligned} \kappa_{ox} &= \kappa_{SiO_2} = 3.9 \\ C_{ox} &= \frac{\kappa_{ox}\epsilon_0}{t_{ox}} \\ &= 1.41 \times 10^{-3}\ \mathrm{F/m^2} \end{aligned} \tag{5.4}$$

$$\begin{aligned} \text{We want;} \qquad C_{ox} &= \frac{\kappa_{oxGaAs}\epsilon_0}{t_{ox}} \\ \text{To do this introduce } t_{ox}^{RC}; \qquad \frac{\kappa_{oxGaAs}\epsilon_0}{t_{ox}} &= \frac{\kappa_{SiO_2}\epsilon_0}{t_{ox}^{RC}} \\ t_{ox}^{RC} &= \frac{\kappa_{SiO_2}}{\kappa_{oxGaAs}} t_{ox} \\ &= 9.13 \times 10^{-9}\ \mathrm{m} \\ &\approx 9\ \mathrm{nm} \end{aligned} \tag{5.5}$$

The junction depth, X_j, can be calculated using equation 5.6, where n_i for GaAs is 2.1×10^6 cm^{-3}, T_{nom} is the temperature (this is one of the BSIM temperature parameters) which is set to 300 K/27° C, and the other parameters are defined as described previously. No ratio correction is required for this value.

$$\begin{aligned} \psi_B &= \frac{k_B T_{nom}}{q} ln\left(\frac{N_s}{n_i}\right) \\ &= 0.63 \text{ V} \\ X_j &= \sqrt{\frac{4\epsilon_{GaAs}\psi_B}{qN_s}} \\ &= 1.512 \times 10^{-7} \text{ m} \end{aligned} \tag{5.6}$$

From the results in chapter 4, we know that the substrate doping (N_s) is 8×10^{16} cm^{-3}. However, by doing a ratio correction on this value we can ensure that the intrinsic carrier concentration (n_i) is correct. n_i is calculated by BSIM as defined by equation 5.7. Where V_{tm0} is the thermal voltage, E_{g0} is the energy bandgap at T_{nom}, and the other parameters are as defined previously. Using these equations the value that BSIM will automatically calculate for n_i ($n_{i_{Si}}$) can be found, as shown in equation 5.8. However, the correct value for n_i in GaAs is 2.1×10^6 cm^{-3}. To achieve this the ratio correction shown in equation 5.9 can be applied to N_s. Where N_s^{RC} is the ratio corrected doping value, which is 5.57×10^{20} cm^{-3}. It is important to note that this is not a physically realistic doping value for GaAs, as the maximum possible doping is approximately 5×10^{19} cm^{-3}. The channel doping (N_{ch}) is also set to N_s^{RC} to ensure that n_i is calculated correctly.

$$\begin{aligned} V_{tm0} &= \frac{k_B T_{nom}}{q} \\ E_{g0} &= 1.16 - \frac{7.02 \times 10^{-4} T_{nom}^2}{T_{nom} + 1108} \\ n_i &= 1.45 \times 10^{10} \left(\frac{T_{nom}}{300.15}\right) exp\left(21.5565981 - \frac{E_{g0}}{2V_{tm0}}\right) \end{aligned} \tag{5.7}$$

$$
\begin{aligned}
V_{tm0} &= \frac{k_B T_{nom}}{q} \\
&\approx 0.026 \text{ V} \\
E_{g0} &= 1.16 - \frac{7.02 \times 10^{-4} T_{nom}^2}{T_{nom} + 1108} \\
&\approx 1.115 \text{ eV} \\
n_i &= 1.45 \times 10^{10} \left(\frac{T_{nom}}{300.15} \right) exp \left(21.5565981 - \frac{E_{g0}}{2V_{tm0}} \right) \\
&= 1.462 \times 10^{10} \text{ cm}^{-3}
\end{aligned}
\tag{5.8}
$$

$$
\begin{aligned}
&\text{We want;} && \frac{N_s}{n_{i_{GaAs}}} = \frac{8 \times 10^{16}}{2.1 \times 10^6} \\
&\text{To do this introduce } N_s^{RC}; && \frac{N_s}{n_{i_{GaAs}}} = \frac{N_s^{RC}}{n_{i_{Si}}} \\
& && N_s^{RC} = 5.57 \times 10^{20} \text{ cm}^{-3}
\end{aligned}
\tag{5.9}
$$

The body-effect coefficients, γ_1 and γ_2, are defined in BSIM as in equation 5.10, these parameters would be automatically calculated if they were not defined. In this case it can be seen that allowing them to be automatically calculated would be insufficient. C_{ox} should be correct due to the ratio correction of t_{ox}. However, N_s and N_{ch} would be incorrect, as they are now both equal to the ratio corrected value N_s^{RC}. By manually calculating as many of the automatically calculated BSIM parameters as possible, a more accurate model can be developed. Equation 5.11 shows how the model values are calculated.

$$
\begin{aligned}
\gamma_1 &= \frac{\sqrt{2q\epsilon_s N_{ch}}}{C_{ox}} \\
\gamma_2 &= \frac{\sqrt{2q\epsilon_s N_s}}{C_{ox}}
\end{aligned}
\tag{5.10}
$$

$$\begin{aligned}\gamma_1 = \gamma_2 &= \frac{\sqrt{2q\epsilon_s N_s}}{C_{ox}} \\ &= \frac{\sqrt{2q\epsilon_{GaAs} N_s}}{\epsilon_{oxGaAs}/t_{ox}} \\ &= 0.454 \text{ V}^{1/2}\end{aligned} \tag{5.11}$$

The doping depth X_t is taken from the Medici simulation structure and is 19 nm. If the bulk to source voltage at which the depletion region width equals the doping depth (V_{bx}), is not given it is calculated by BSIM using equation 5.12. As with γ_1 and γ_2 allowing V_{bx} to be automatically calculated would be insufficient, as N_s is now equals the ratio corrected value N_s^{RC}, which will give an incorrect result. Equation 5.13 shows the correct model values. Where ψ_B is as previously calculated, and the doping and carrier concentration values are the correct physical values for the GaAs devices.

$$\begin{aligned}V_{bx} &= \psi_s - \frac{qN_s X_t^2}{2\epsilon_s} \\ \psi_s &= 2\psi_B = 2\frac{k_B T_{nom}}{q} ln\left(\frac{N_s}{n_i}\right)\end{aligned} \tag{5.12}$$

$$\begin{aligned}\psi_s &= 2\psi_B = 2\frac{k_B T_{nom}}{q} ln\left(\frac{N_s}{n_i}\right) \\ &= 1.26 \text{ V} \\ V_{bx} &= \psi_s - \frac{qN_s X_t^2}{2\epsilon_{GaAs}} \\ &= 1.24 \text{ V}\end{aligned} \tag{5.13}$$

5.4.2 DC Parameters

This section details the calculations for the DC parameters. The key parameters in this section include the threshold voltage (V_{th}), flat-band voltage (V_{fb}), mobility (μ_{eff}) and the parasitic resistances and capacitances (R_{dsw}, R_{sh} and C_{dsc}). Table 5.2 shows all of the relevant GaAs values. Calculations for these follow, along with any necessary ratio corrections. The BSIM DC parameters that are not listed in table 5.2 are taken to be the BSIM defaults, these can be found in appendix E.

Table 5.2: BSIM3v3.2 DC Values

Symbol Used in Equations	Symbol Used in SPICE	GaAs Value	Ratio Corrected Value
V_{th}	vth0	-0.93 V (PMOS) 0.93 V (NMOS)	no RC
K_1	k1	0.454 $V^{1/2}$	no RC
K_2	k2	0	no RC
V_{fb}	vfb	-2.387 V (PMOS) -0.527 V (NMOS)	no RC
μ_0	u0	240 cm^2/Vs (PMOS) 1500 cm^2/Vs (NMOS)	no RC
μ_a	ua	0.53×10^{-8} m/V (PMOS) 0.1×10^{-8} m/V (NMOS)	no RC
μ_b	ub	0 $(m/V)^2$	no RC
μ_c	uc	0 m/V^2	no RC
V_{sat}	vsat	1×10^5 m/s	no RC
a_0	a0	1	0.199
R_{dsw}	rdsw	1.05×10^3 $\Omega - \mu$m	no RC
N_{factor}	nfactor	1	0.012
C_{dsc}	cdsc	6.15×10^{-3} F/m^2	no RC
P_{clm}	pclm	1	no RC
D_{rout}	drout	0.56	0.0613
R_{sh}	rsh	1234 Ω/sq	no RC

The threshold voltage, V_{th}, is known, as discussed in chapter 4. It is -0.93 V for the PMOS device and taken to be 0.93 V for the NMOS device.

K_1 and K_2 are calculated from the BSIM equations shown in equation 5.14. They

are the first and second order body effect coefficients, respectively. Where γ_1 and γ_2 are as defined in equation 5.11, ψ_s is defined as in equation 5.13, V_{bx} is defined as in equation 5.13, and V_{bm} is the maximum applied body bias. As $\gamma_1 = \gamma_2$, K_2 is zero. As K_2 is zero, $K_1 = \gamma_2 = 0.454\ V^{1/2}$.

$$\begin{aligned} K_1 &= \gamma_2 - 2K_2\sqrt{\psi_s - V_{bm}} \\ K_2 &= \frac{(\gamma_1 - \gamma_2)\left(\sqrt{\psi_s - V_{bx}} - \sqrt{\psi_s}\right)}{2\sqrt{\psi_s}\left(\sqrt{\psi_s - V_{bm}} - \sqrt{\psi_s}\right) + V_{bm}} \end{aligned} \tag{5.14}$$

The flat band voltage value, V_{fb}, does not need to be defined as BSIM will automatically calculate this, and unlike some of the other parameters this will be the correct value. Equation 5.15 shows how V_{fb} is calculated. V_{th} is known, and K_1 is as defined above. ψ_s is as defined in equation 5.13, this is internally calculated by BSIM and will be the correct value as T_{nom} has been defined and N_s has been defined as the ratio corrected value.

$$\begin{aligned} V_{fb} &= V_{th} - \psi_s - K_1\sqrt{\psi_s} \\ &= -2.387\ \text{V (PMOS)} \\ &= -0.527\ \text{V (NMOS)} \end{aligned} \tag{5.15}$$

As shown in sections 4.4.3 and 4.5 the mobility of the majority charge carriers can be found from the Medici simulations. As BSIM is unable to replicate the GaAs-like mobility curve these fixed values were used to approximate what had been observed in the Medici models. The mobility μ_{eff} is calculated by BSIM using equation 5.16, as mobility model 1 has been chosen in the model control parameters (mobMod = 1). μ_0 is the mobility at temperature T_{nom}. This is set to be 240 cm^2/Vs for the PMOS device and 1500 cm^2/Vs for the NMOS device. V_{gsteff} is the effective V_{gs} - V_{th} which is calculated internally, it will be calculated correctly due to corrections to the parameter N_{factor}. V_{bseff} is the effective bulk to source voltage, this is correctly calculated internally. μ_a and μ_b are the first and second order mobility degradation coefficients, respectively, and μ_c is the body-effect mobility degradation coefficient. The second order effects are neglected, so μ_b and μ_c are set to zero. μ_a was adjusted

to achieve a good fit with results. This was done using part of the Aurora parameter extraction software, which allows the user to slide the value of a variable and show how this effects the curve fitting.

$$\mu_{eff} = \frac{\mu_0}{1 + (\mu_a + \mu_c V_{bseff}) \left(\frac{V_{gsteff}+2V_{th}}{t_{ox}}\right) + \mu_b \left(\frac{V_{gsteff}+2V_{th}}{t_{ox}}\right)^2} \tag{5.16}$$

As mentioned above the parameter N_{factor}, which is the sub threshold swing factor, is set to insure that V_{gsteff} is correct. This is due to the fact that the calculation for V_{gsteff} contains the parameter n, whose equation in turn contains N_{ch} outside the desired ratio, N_{ch}/n_i. It appears as $\sqrt{N_{ch}}$ and is multiplied by N_{factor}. So to effectively still get the default value for N_{factor}, which is the best approximation, N_{factor}^{RC} is calculated as shown in equation 5.17.

$$\begin{aligned} N_{factor}^{RC}\sqrt{N_{ch}^{RC}} &= N_{factor}\sqrt{N_{ch}} \\ N_{factor}^{RC} &= \frac{N_{factor}\sqrt{N_{ch}}}{\sqrt{N_{ch}^{RC}}} \qquad \text{Where } N_{factor} = 1 \\ &= 0.012 \end{aligned} \tag{5.17}$$

The saturation velocity, V_{sat}, is set to 1×10^5 m/s [7, 10]. This is the is the value for InGaAs, which is the channel material. The parasitic contact resistance (R_{dsw}) and source drain sheet resistance (R_{sh}) are know to be 1.05 $\times$ 10^3 Ω-μm and 1234 Ω/sq respectively, as discussed in section 4.4.1.

Similarly to N_{factor}, a_0 (the bulk charge effect coefficient for channel length), D_{rout} (length dependence coefficient of the DIBL correction parameter for the parameter Rout) and D_{sub} (DIBL coefficient exponent in the sub threshold region) are used to fix second order ratio correction errors.

The channel length modulation parameter (P_{clm}) is set to 1, as the characteristic data is limited to 0.6 μm gate length.

C_{dsc} is the drain/source to channel coupling capacitance, as shown in equation 5.18. t_{dsc} is the thickness between the source/drain and the channel. This is includes a 0.5 nm thick layer of GaAs (κ_{GaAs} = 13.1) and 15 nm of AlGaAs (κ_{AlGaAs} = 10.7). Using equation 5.1, it can be shown that t_{dsc} equals 15.5 nm, and κ_{dsc} equals

10.79. Hence, C_{dsc} equals 6.15×10^{-3} F/m^2. This value was also confirmed using Medici simulations.

$$\begin{aligned} C_{dsc} &= \frac{\epsilon_{dsc}}{t_{dsc}} \\ &= \frac{\kappa_{dsc}\epsilon_0}{t_{dsc}} \\ &= 6.15 \times 10^{-3} \text{ F/m}^2 \end{aligned} \tag{5.18}$$

5.4.3 C-V Model Parameters

This section details the calculations for the C-V parameters. The key parameters in this section include the overlap and junction capacitances in the device. Capacitance model 3 (capMod = 3) was used. This was introduced in BSIM3v3.2 as a new intrinsic capacitance model. It considers the finite charge layer thickness, determined by quantum effects, and is very accurate in all operating regions [80]. Table 5.3 shows all of the relevant GaAs values, calculations for these follow. The BSIM C-V parameters that are not listed in table 5.3 are taken to be the BSIM defaults, these can be found in appendix E.

Table 5.3: BSIM3v3.2 C-V Model Values

Symbol Used in Equations	Symbol Used in SPICE	GaAs Value
X_{part}	xpart	1
C_{gs0}	cgs0	3.45×10^{-10} F/m
C_{gd0}	cgd0	3.45×10^{-10} F/m
C_j	cj	7.7×10^{-4} F/m^2
C_κ	ckappa	0 F/m
C_f	cf	0 F/m
CLC	clc	0 m
CLE	cle	1
acde	acde	9.14 m/V

X_{part}, the charge partitioning flag, can be used to select the one of three different charge partitioning schemes. These represent the ratios of the drain charge (Q_d) to

the source charge (Q_s) in the saturation region. The available ratios are 0/100, 50/50 and 40/60, and are represented by $X_{part} = 0$, 0.5 and 1, respectively. $X_{part} = 1$ was chosen as this represents the most physical partitioning scheme. The channel charges are allocated to the source and drain terminals by assuming a linear dependence in the y direction [80].

C_{gs0} (non lightly doped drain region, source to gate overlap capacitance per channel length), would be calculated by BSIM as shown in equation 5.19. As with the other parameters, where there is an option to enter the value rather than allow the automatic calculation, this is done. This helps to ensure that all of the correct physical values are used. DLC is the length offset fitting parameter from C-V, the default value for this is L_{int} (the length offset fitting parameter from I-V without bias) which has been set to the default of zero. The result is shown in equation 5.20, where X_j and C_{ox} are as calculated previously. C_{gd0} (non lightly doped drain region, drain to gate overlap capacitance per channel length), is calculated in a similar way to C_{gs0}.

$$\begin{aligned}
&\text{if (DLC is given and is greater than 0) then} \\
&\quad C_{gs0} = DLC \times C_{ox} - C_{gs1} \\
&\quad \text{if } (C_{gs0} < 0) \text{ then } C_{gs0} = 0 \\
&\text{else} \\
&\quad C_{gs0} = 0.6X_j \times C_{ox}
\end{aligned} \tag{5.19}$$

$$\begin{aligned}
C_{gs0} &= 0.6X_j \times C_{ox} \\
&= 3.45 \times 10^{-10} \text{ F/m}
\end{aligned} \tag{5.20}$$

The junction capacitance, C_j, is calculated as shown in equation 5.21. Where X_j is the junction depth as calculated previously.

$$\begin{aligned}
C_j &= \frac{\epsilon_j}{X_j} \\
&= \frac{\kappa_{GaAs}\epsilon_0}{X_j} \\
&= 7.7 \times 10^{-4} \text{ F/m}^2
\end{aligned} \tag{5.21}$$

C_κ, the coefficient for lightly doped region overlap capacitance, only appears in equations where another parameter zeros that part of the equation, so it is not used and is therefore set to zero.

C_f is the fringing field capacitance. The BSIM equations for this would be inaccurate as they use the thickness of the poly silicon in the equation. It was decided that the effects of this would be negligible as the device has a long gate length (0.6 μm) and large width (10 μm), relative to the thickness of the oxide (24.5 nm) [82].

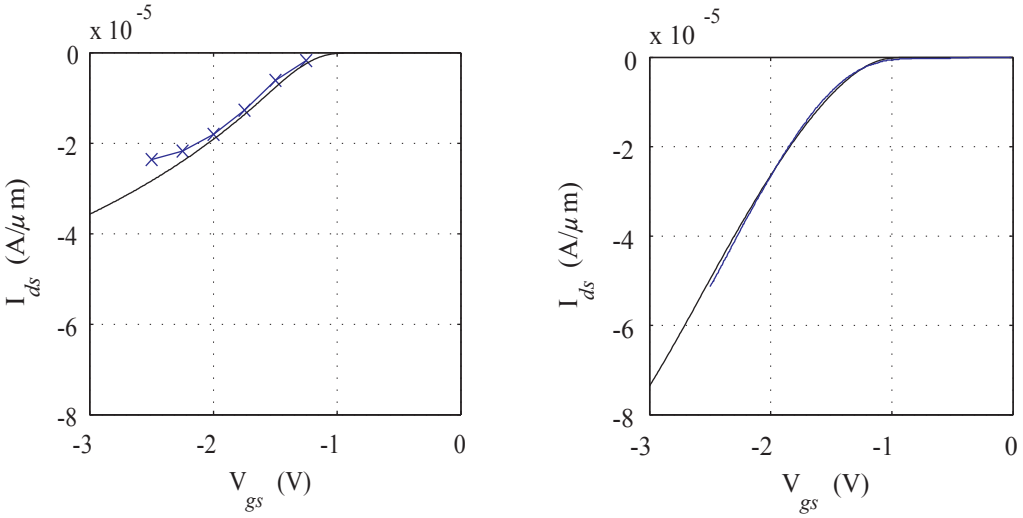
As the short channel model was not required in this case, CLC (constant term for the short channel model) and CLE (exponential term for the short channel model) were set to 0 and 1 respectively to switch this off.

The parameter acde (default value 1) is the exponential coefficient for charge thickness for accumulation and depletion regions. This parameter was used to implement second order numerical corrections. It appears in calculations for the DC charge thickness, where ratio corrections were insufficient to correct for all of the parameters.

5.5 Results and Discussion

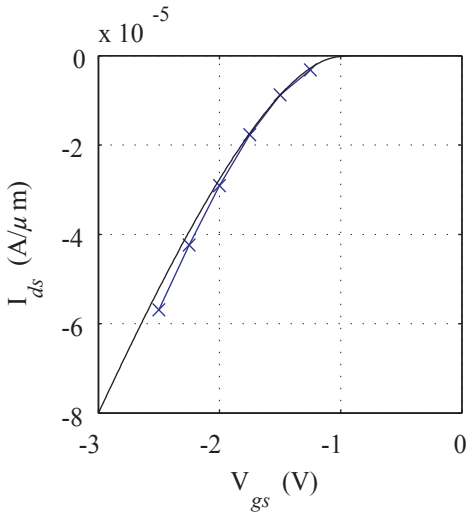
As in the previous chapter the goal was to create models which are well calibrated to the measured data, this time in the form of BSIM3v3.2 compact models. It can be seen from figures 5.3 and 5.4 that this was achieved. The results of the investigations in the previous chapter were essential in this process. The NMOS compact model can also been seen to be calibrated to the drift-diffusion results, as shown in figure 5.5.

As described in the sections above, the method for creating the compact models centered around adapting the Si/SiO_2 BSIM3v3.2 model to make it physically relevant for $GaAs/Ga_2O_3$ devices. To achieve this, a ratio correction technique was used to allow indirect access to fundamental physical parameters that are otherwise inaccessible in the BSIM3v3.2 model. This method could be applied to future GaAs devices, and to other unconventional MOS devices that have yet to be well established and have their own versions of compact models available.



(a) V_{ds} = -0.5 V

(b) V_{ds} = -1.5 V



(c) V_{ds} = -2.5 V

Figure 5.3: PMOS gate characteristics - BSIM Cadence Spectre results (black) compared to the Motorola measured results (blue).

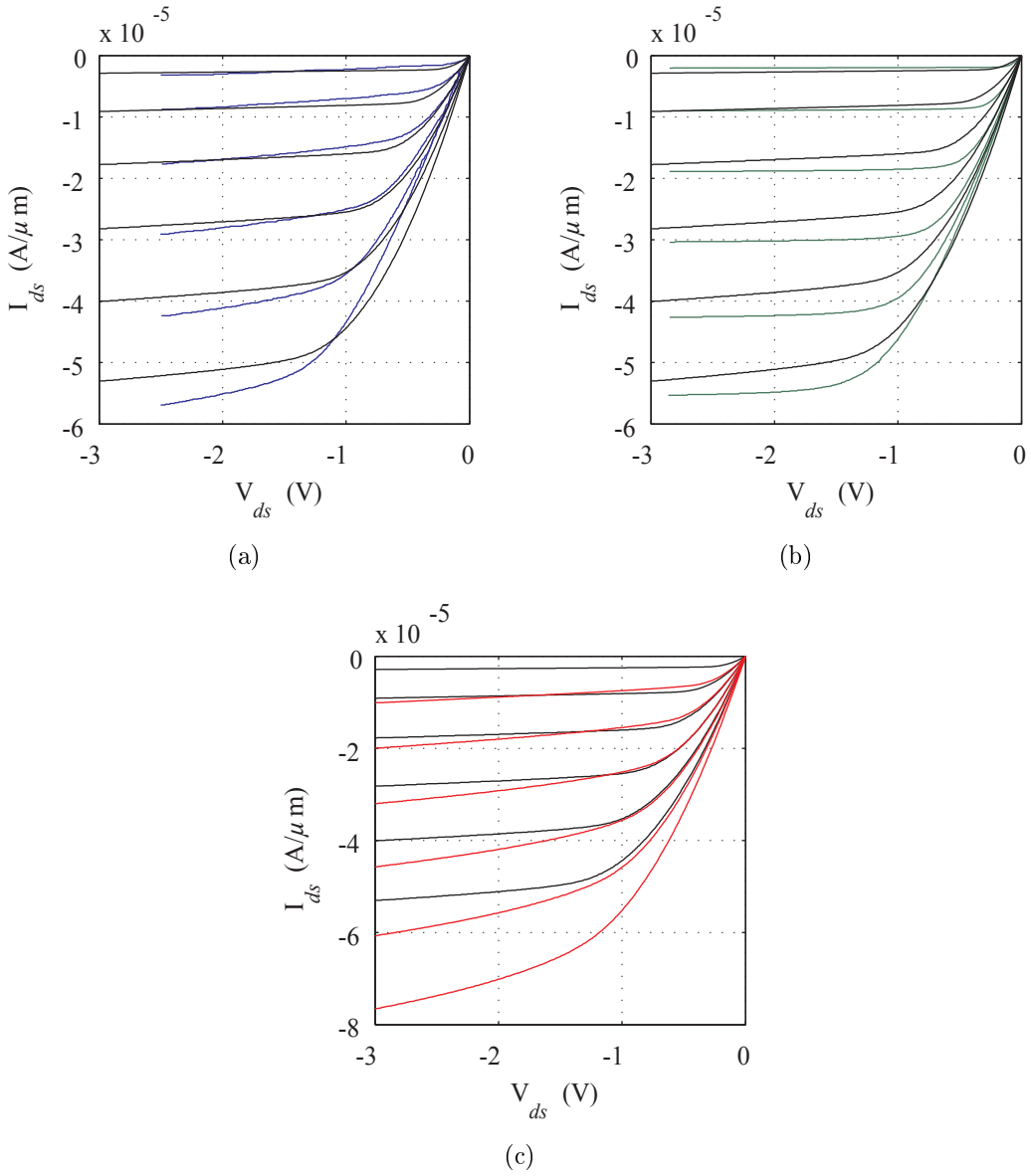


Figure 5.4: PMOS drain characteristics, where $-2.5V \leq V_{gs} \leq -1.25V$ at 250 mV intervals for each family of curves. (a) BSIM Cadence Spectre results (black) compared to the Motorola measured results (blue). (b) BSIM Cadence Spectre results (black) compared to the Medici drift-diffusion results (green). (c) BSIM Cadence Spectre results (black) compared to a similarly-sized silicon device (red).

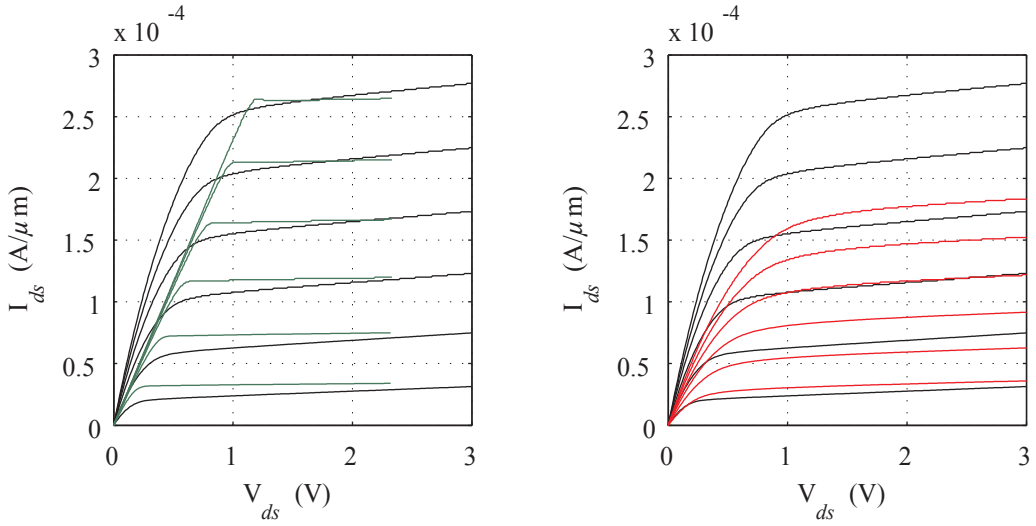


Figure 5.5: NMOS drain characteristics, where $1.25V \leq V_{gs} \leq 2.5V$ at 250 mV intervals for each family of curves. (a) BSIM Cadence Spectre results (black) compared to the Medici drift-diffusion results (green). (b) BSIM Cadence Spectre results (black) compared to a similarly-sized silicon device (red).

5.6 Summary

In this chapter, BSIM3v3.2 compact models have been developed and calibrated based on measured data and the drift-diffusion models described in chapter 4. Results have been presented that show that the compact models are well matched to these characteristics. As with the drift-diffusion models, the calibration of these models could be further improved in the future if more measured device data was available.

BSIM model equations, and MOSFET theory, were used to calculate the GaAs BSIM parameters. However, it was necessary to thoroughly investigate the parameter dependencies within the BSIM model to find instances where the model would make incorrect assumptions. This is due to inaccessible physical parameters, such as permittivities and intrinsic carrier concentrations of materials, which are set to the Si/SiO_2 values. Hence, the technique of ratio correction was introduced to adjust the calculated GaAs values to allow for this. Additionally, as BSIM cannot include information on complex dielectric stacks, some approximations had to be

made using effective medium theory.

In the next chapter, the compact models will be imported into circuit design tools to investigate the potential circuit performance of this technology in different circuit styles.

6 Digital Circuit Design

6.1 Introduction

Following the successful development of BSIM models for GaAs/Ga_2O_3 MOSFETS in chapter 5, the models were then used to investigate the potential performance and attributes of GaAs digital circuits. This is achieved by examining a range of different circuit styles. CMOS is used as a benchmark, however due to the properties of GaAs this was not expected to be the most efficient style to use. The properties of a 0.6 μm CMOS inverter in silicon (the 0.6 μm Austria Microsystems process is used, see appendix C for the BSIM model) and GaAs are thoroughly investigated and then the benefits of using alternative styles are discussed. Then the sub components of an 8-bit carry select adder are used as an example to compare performance between silicon and GaAs, and between the various design styles in each technology.

6.2 Integrating BSIM Models with Circuit Design Tools

BSIM3v3.2 models can be easily integrated with circuit design tools, including Cadence Integrated Circuit. Cadence's SPICE simulator Spectre can either be accessed using the graphical schematic editor (Virtuoso Schematic Editing and Analog Design Environment) or by writing a netlist to describe the circuit and executing this via a command line interface.

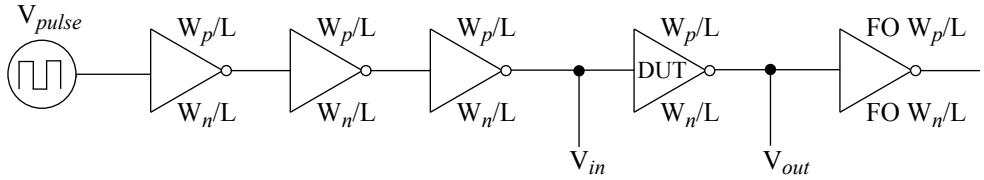
The results in this work were generated using the graphical interface, as this has various functions that are not available via the command line. These included among others the use of the *calculator* function in Cadence, which allows the user to set up calculations and plot their results. Calculations can be based on the basic graphable outputs from a circuit simulation, such as the voltages and currents in the circuit. This is particularly useful when doing a parametric analysis, where a simulation (for example, transient) might be run several times with different circuit parameters (for example, one of the transistor widths). A circuit characteristic (such at rise time, t_r) can be calculated for each variation and then plotted against the parameter that was varied (the transistor width). This feature was used extensively in section 6.6 to complete the circuit simulation and analysis.

To integrate my BSIM models successfully the following steps are followed;

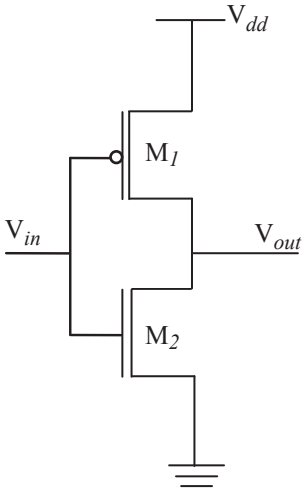
- Start Cadence Mixed-Signal Front-to-Back Design (msfb).
- Start a new library and link to the AMS 0.6 μm technology.
- Ensure the device names in my model card match AMS (this explains the choice of calling the devices modn and modp in appendix F). This means that the AMS symbols can be used to draw the schematic and this will also match up to my models.
- Create the schematic in Virtuoso Schematic Editing using the devices in the AMS technology library (PRIMLIB).
- Set up the simulation in Virtuoso Analog Design Environment. This includes setting the inputs, supply voltage, and simulation type.
- In Setup/Model Libraries,
  - to run with AMS 0.6 μm leave the defaults (as in appendix C).
  - to run with my GaAs models disable the AMS default models, and add and enable my model card file (as in appendix F).

6.3 CMOS Inverter

CMOS (complementary MOS) is so named due to its complementary structure which utilises both equal numbers of PMOS and NMOS transistors. The total number of transistors for a logic function is 2N, where N is the number of inputs. There is no static power consumption when using CMOS and the noise margins are usually better than the alternative circuit styles that will be discussed in section 6.4. Due to the lower mobility of the charge carriers (holes) in the channel of PMOS devices compared to the charge carrier (electron) mobility in the NMOS devices, device width scaling has to be used to make sure that the pull-up provided by the PMOS device is sufficient. When designing with silicon CMOS it is usual for the widths of the PMOS devices to be two to three times that of the NMOS devices. This effect is exaggerated in the case of GaAs CMOS as the mobility ratio of electrons/holes



(a) Test Circuit.



(b) Individual CMOS Inverter.

Figure 6.1: CMOS Inverter Test Circuit for Timing Characteristics. L = 0.6 μm, W_n = 10 μm, W_p = W_n tSize, and V_{dd} = 3 V.

is much larger in GaAs than silicon. Therefore it is expected that CMOS will not be the ideal circuit style to use for GaAs digital logic, however it provides a necessary benchmark for comparison with results in other styles. In this section, silicon and GaAs CMOS inverters are compared. In section 6.6 1-bit adders and 2-input multiplexers in various circuit styles, in both silicon and GaAs, will be compared.

First the timing characteristics of an inverter were investigated, the circuit used for this was as shown in figure 6.1(a). The internal structure of the inverters is as shown in figure 6.1(b). This was set up in the Cadence Analogue Design Environment as described in section 6.2. The device-under-test (DUT) is the fourth inverter in the chain of five. There are two reasons for this: First, this insures that the waveform being input to the DUT is realistically distorted rather than a perfect square wave. The second is that the fifth inverter acts as a realistic load for the

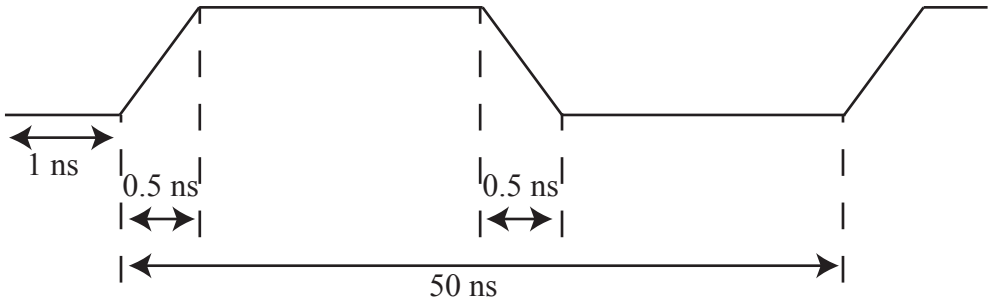


Figure 6.2: Input test signal for CMOS timing analysis.

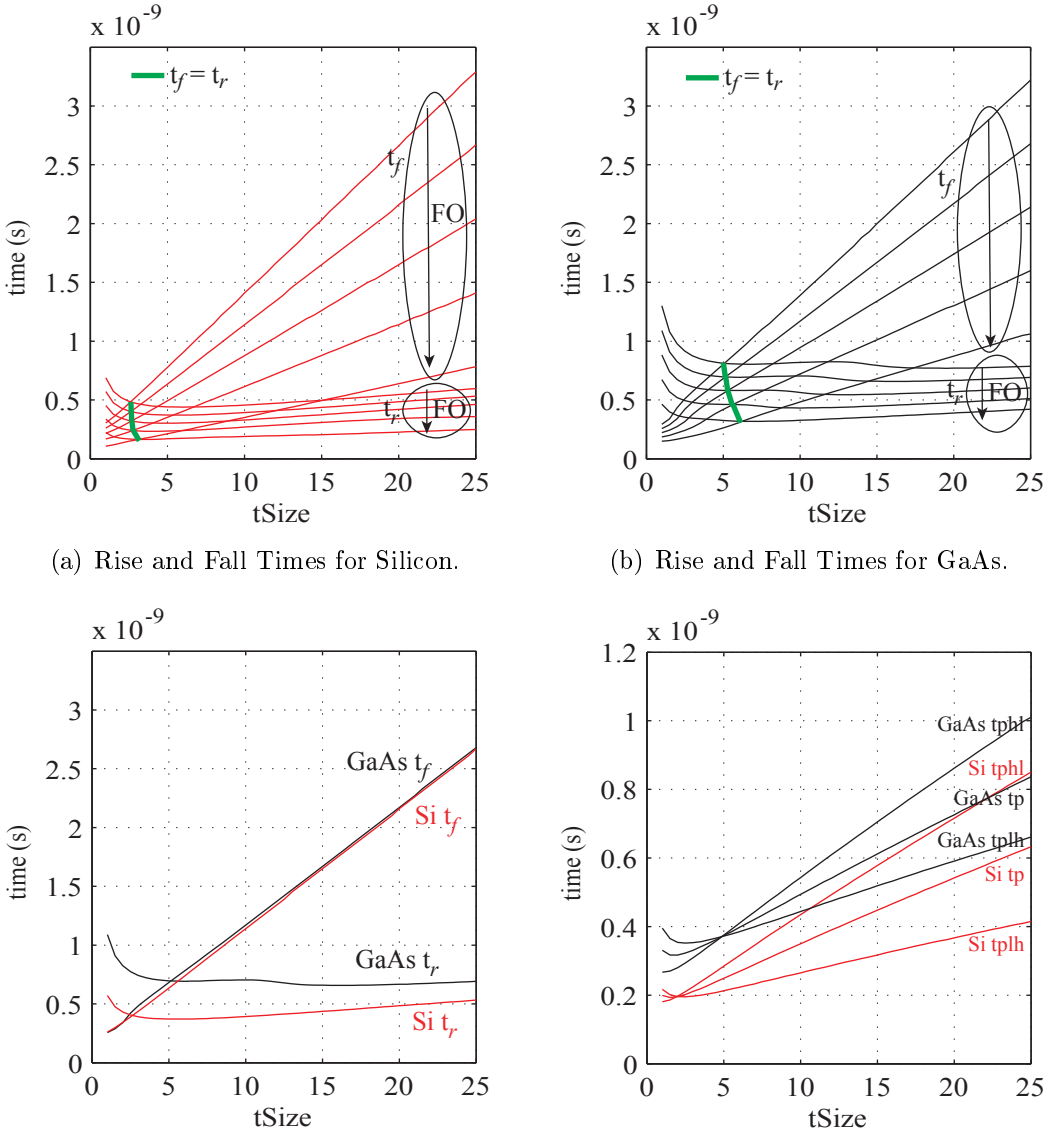
DUT. The input test signal (V_{pulse}) was as shown in figure 6.2.

The gate length of all of the MOSFETs is L = 0.6 μm, the width of the NMOS devices is W_n = 10 μm, the width of the PMOS devices is $W_p = W_n$ tSize, and the supply voltage is V_{dd} = 3 V. The variable tSize is the ratio W_p/W_n, which is expected to be larger for optimum performance in the GaAs circuit compared to the silicon one. The width of both of the MOSFETs in the final inverter are multiplied by *FO*, which represents the fan-out attached to the output of the DUT. Fan-out is the number of different devices or gates that are attached to the output, the higher the fan-out the greater the load on the gate. Results were generated for various tSizes and FOs, and are shown in figure 6.3.

If we consider the rise (t_r) and fall (t_f) times of V_{out} from 10-90% for silicon and GaAs, a good approximation for the optimum tSize is where the rise and fall times are equal. This point varies slightly with the fan-out, however from figure 6.3(a) it can be seen that the optimum tSize-ing is ≈ 2.5 for silicon as expected. From figure 6.3(b) it can be seen that for GaAs it is closer to 5.

A typical fan-out in an integrated circuit is 4 [83], so in figure 6.3(c) values for silicon and GaAs are compared with the same fan-out. In this case the optimum tSize for silicon is 2.5, and 5 for GaAs. In figure 6.3(d) the time to propagate a high-to-low (tphl) and low-to-high (tplh) input signal are also compared. The average of these is also shown (t_p). This is taken as the time that is takes the input at V_{th} to propagated to the output. V_{th} is calculated using the circuit shown in figure 6.4(a), the values for V_{th} are as shown in figure 6.4(b).

It can be seen both the rise and fall times and the propagation delays are longer



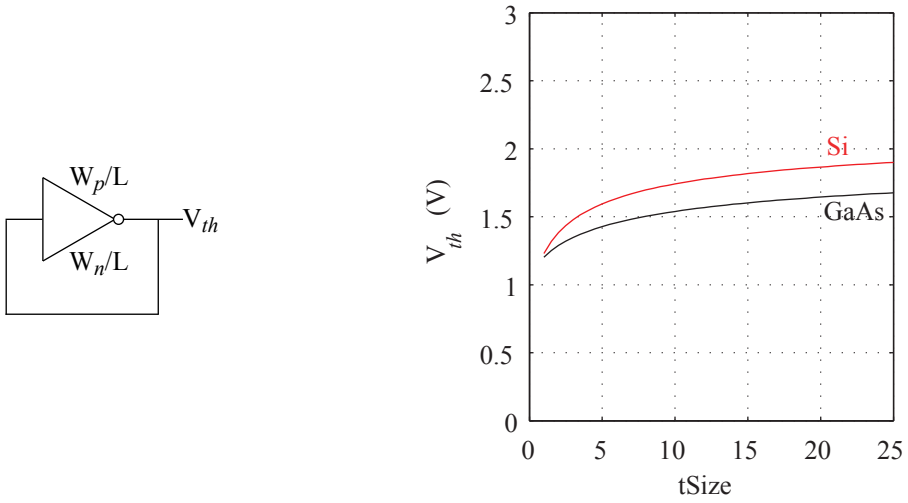
(a) Rise and Fall Times for Silicon.

(b) Rise and Fall Times for GaAs.

(c) Rise and Fall Times when FO = 4.

(d) Propagation Delay Times when FO = 4.

Figure 6.3: Inverter Timing Characteristics.



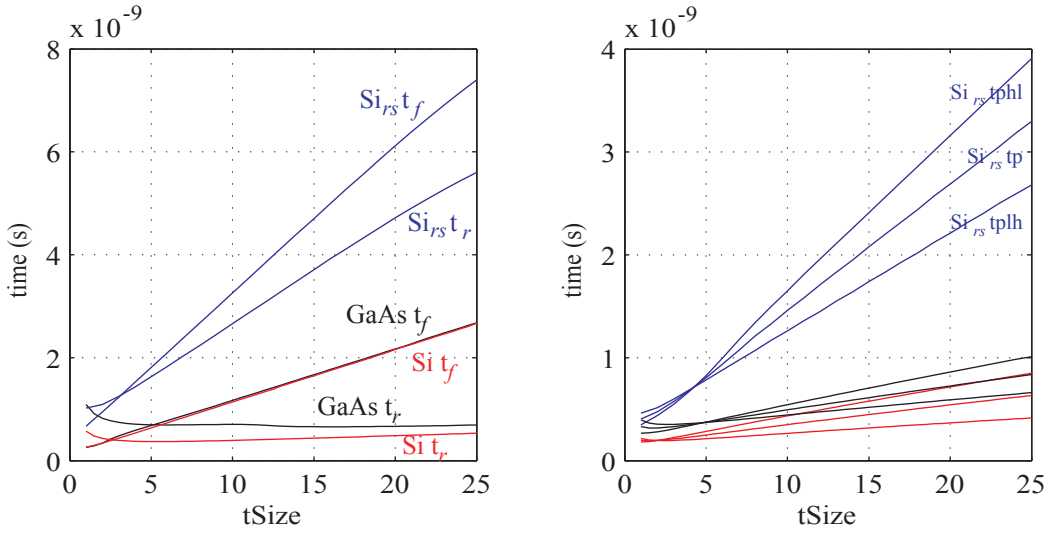
(a) Test Circuit. (b) Threshold Voltage.

Figure 6.4: Inverter Threshold Voltage Circuit and Results. L = 0.6 μm, W_n = 10 μm, W_p = W_n tSize, and V_{dd} = 3 V.

for the GaAs circuit. This can mainly be attributed to the higher access resistance in the GaAs device. To demonstrate this, artificial additional resistance was added to the sources of the PMOS and NMOS devices in the silicon version of the DUT. The results of adding 1 kΩ resistors are shown in figure 6.5. It can be seen that all of the delay times have increased.

The longer delay times in GaAs might also be partially attributed to the fact that the higher electron velocity in GaAs is a consequence of a lighter electron effective mass. This effect is especially pronounced in short channel devices where ballistic and overshoot effects play a dominant role [7]. So, it is likely in future smaller gate length GaAs devices, that improvements will be seen. When this data is available the methodologies presented in this thesis can be re-used to see if this is the case.

Next the static characteristics of an inverter were investigated. Figure 6.6(a) shows the test circuit used for this. This circuit was used to generate the results in figures 6.6(b) and 6.6(c). Figure 6.6(b) shows the transfer characteristics for silicon and GaAs inverters when $W_p = W_n$. Figure 6.6(c) shows the transfer characteristics for silicon and GaAs inverters when $W_p = W_n$ tSize, where tSize is the optimum for each technology, which is 2.5 for silicon and 5 for GaAs.



(a) Rise and Fall Times when FO = 4. (b) Propagation Delay Times when FO = 4.

Figure 6.5: Inverter Timing Characteristics. The black and red curves are GaAs and silicon respectively and are the same as in figure 6.3(c) and 6.3(d). The blue curves are silicon with the addition of a 1 kΩ resistor on the source of each transistor in the device under test.

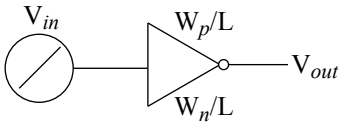
The noise margins shown in figure 6.6(d) are calculated from transfer characteristics for tSizes from 1 to 25. Noise margins are calculated as shown in figure 6.7 and equation 6.1. The points (V_{IL}, V_{OH}) and (V_{IH}, V_{OL}) are identified by taking the derivative of the transfer characteristics. Where the derivative equals -1 this indicates the data points.

$$NMH = V_{OH} - V_{IH} \tag{6.1a}$$

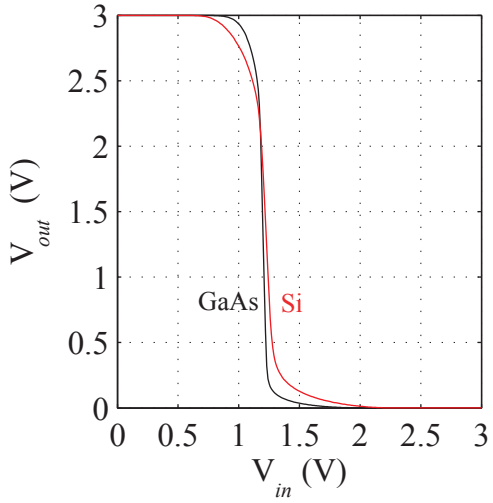
$$NML = V_{IL} - V_{OL} \tag{6.1b}$$

$$NM = \frac{NMH + NML}{2} \tag{6.1c}$$

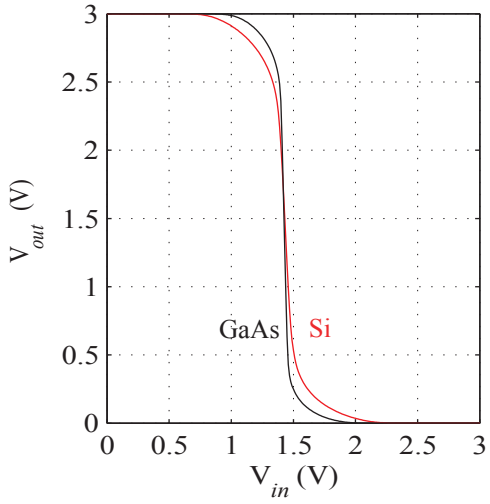
It can be seen from figure 6.6(d) that the noise margin high (NMH) is always better in the GaAs circuit than in the silicon one. However, the noise margin low (NML) is only better in the GaAs circuit at tSizes less than 2.5. The average noise margin (NM) is always better in the GaAs circuit than the silicon one.



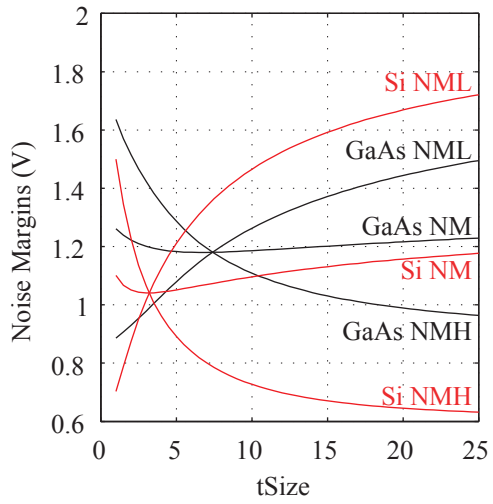
(a) Test Circuit.



(b) Transfer Characteristics when tSize = 1.



(c) Transfer Characteristics when tSize = 2.5 for Si and tSize = 5 for GaAs.



(d) Noise Margins.

Figure 6.6: Inverter Static Characteristics. L = 0.6 μm, W_n = 10 μm, $W_p = W_n$ tSize, and V_{dd} = 3 V.

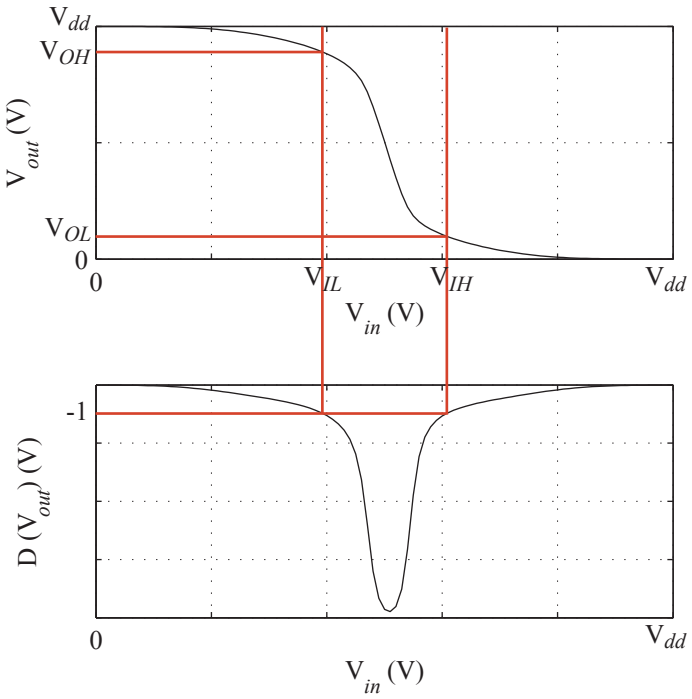


Figure 6.7: Method for calculating the noise margins from a transistors transfer characteristics.

6.4 Alternative Circuit Styles for GaAs Digital Logic

As mentioned previously it was not expected that CMOS would provide the best circuit style for GaAs digital design. The key issue with CMOS is that in having a complimentary structure there are as many PMOS devices as NMOS devices, this at the very least will mean more area for a circuit designed in this style in GaAs compared to silicon. However, as the PMOS devices in GaAs actually perform worse than silicon it makes sense to use as few as possible. Which means that alternative circuit styles must be considered.

In this section a summary of alternative circuit styles which have either a reduced number of PMOS devices, or use none at all, will be given and their attributes discussed. In section 6.6 some of these styles are selected to compare their benefits when implemented in both silicon and GaAs circuits.

6.4.1 Resistively Loaded NMOS

Resistively loaded NMOS requires only NMOS devices, as a resistor is used to provide the pull-up in the circuit. A schematic of an inverter circuit in this style is shown in figure 6.8(a). The number of devices required is equal to the number of inputs (N). There are several problems associated with this logic style: The noise margins are poor. There is static current (or leakage) as the low output voltage (V_{OL}) is not zero volts, thus adversely effecting power consumption. Finally, resistors take up a large area on a chip. The larger the resistor in this circuit the lower the static current and the higher the rise time for the output, therefore trade offs must be made when using this architecture.

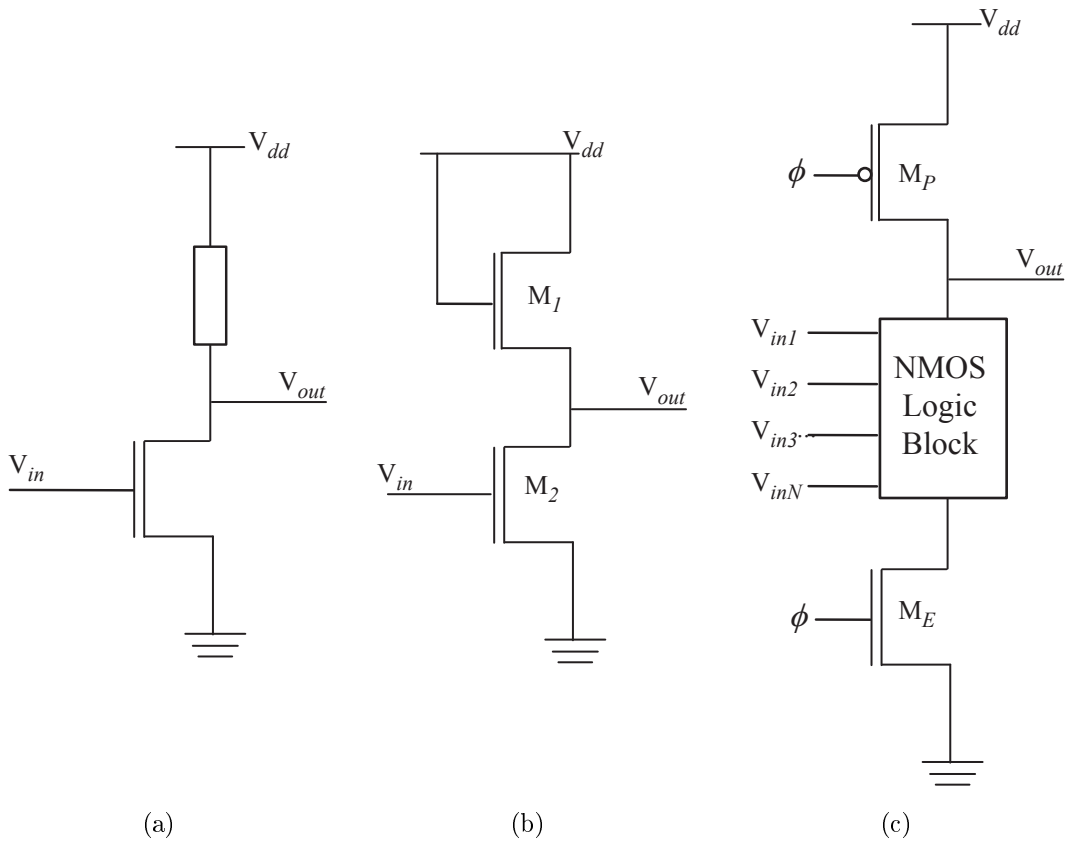


Figure 6.8: Logic Styles Investigated for GaAs Digital Circuits. (a) Resistively Loaded Inverter. (b) NMOS Saturated Enhancement Load Inverter. (c) Generic N-block Precharge Logic Gate.

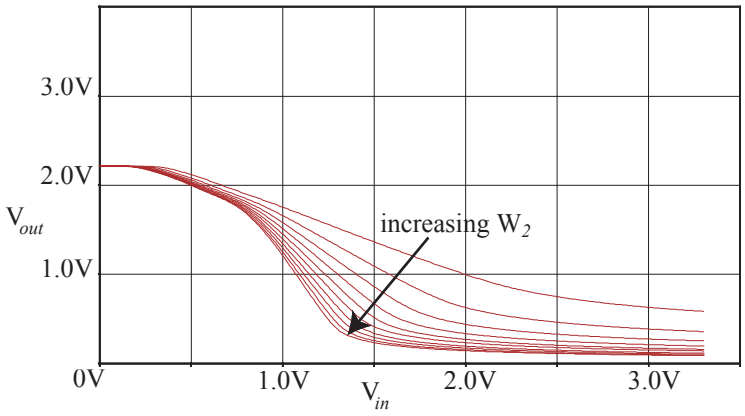


Figure 6.9: Transfer characteristics for a saturation enhancement load inverter. V_{dd} = 3.3 V. 1 μm $\leq W_2 \leq$ 10 μm, where W_2 is the width of M_2 as shown in figure 6.8(b). $L_1 = L_2 = W_1 = 1$ μm.

6.4.2 NMOS Saturated Enhancement Load

The NMOS saturated enhancement load circuit style also allows circuits to be design using only one transistor type. The number of devices required is the number of inputs plus one (N + 1). For an example circuit of an NMOS saturated enhancement load inverter see figure 6.8(b). To extend this inverter model to other logic functions the pull down network is designed as CMOS but the pull up network is replaced with a single NMOS device connected as M_1 in figure 6.8(b). This circuit style has the advantage compared to the resistively loaded circuit that it takes up less area. However it also suffers from the static current problem and the noise margins are low.

Figure 6.9 shows the transfer characteristics of an NMOS saturated enhancement load inverter with different transistor size ratios. As the width of M_2 (W_2) is increased, V_{OL}, and therefore the static current, is reduced. So, by correctly sizing the pull down transistors in the circuit the characteristics can be improved.

The output high voltage V_{OH} of this style of circuit is less easy to improve and therefore the static current issue cannot be removed entirely. For example, if the width of M_1 is increased V_{OH} increases but so does V_{OL}. It was found that the increase in V_{OH} was relatively small compared to the increase in V_{OL} and therefore it is best to keep the width of M_1 equal to its length, with regard to the static

current.

6.4.3 NMOS Precharge

NMOS precharge logic is like designing a block in CMOS and then discarding the PMOS block. Contrary to the behaviour of CMOS, precharge logic is dynamic and requires two additional clocked transistors, one PMOS and one NMOS. Dynamic logic relies on stored charge in the parasitic capacitances of the circuit nodes for correct operation, and needs to be periodically refreshed to avoid charge leakage [84].

A generic NMOS precharge circuit, is shown in figure 6.8(c). This type of logic requires the number of inputs plus one NMOS transistors and one PMOS transistor (N + 2). So, the more complex the circuit the greater the return on area compared to CMOS (if the number of inputs is greater than two, precharge circuits use less transistors). Also only as only one PMOS device is required this has obvious advantages for the GaAs paradigm. Additionally, the noise margins and static current are better for precharge logic, than for the NMOS saturated enhancement load circuits discussed previously.

A transient analysis of a precharge inverter is shown in figure 6.10 to illustrate how precharge gates operate. When the clock signal (ϕ) is low this is the precharge region and the output is high. When the clock is high this is the evaluation region and the output of the gate will be logically valid. This can be seen in figure 6.10, figure 6.10(a) is the clock signal, figure 6.10(b) shows a steady low input signal and 6.10(c) is the corresponding output. Figure 6.10(d) shows a steady high input signal and 6.10(e) is the corresponding output. A change in the input during the precharge region will not be reflected until the clock switches and we enter the evaluation region, unless of course this change means that the output will logically be high.

6.4.4 NMOS Precharge with Enhancement Load

A possible hybrid combining precharge logic and enhancement load is another possible design solution. An example of a suggested inverter circuit is shown in figure 6.11.

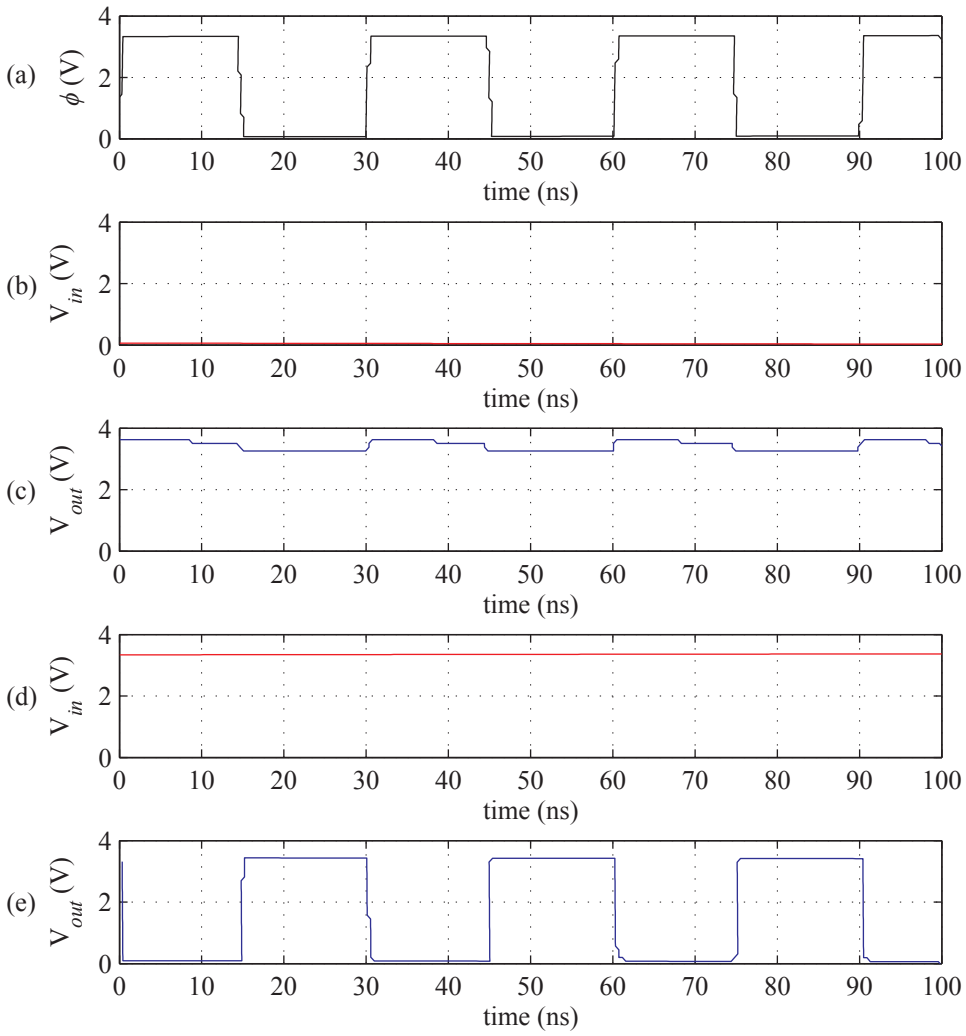


Figure 6.10: Precharge inverter transient analysis. V_{dd} is 3.3 V. L = W = 1 μm in all MOSFETs. (a) is the clock signal ϕ. (b) shows the input as low and (c) shows the resultant V_{out} for this. (d) shows the input as high and (e) shows the resultant V_{out} for this.

In this circuit V_{OH} is lower and V_{OL} is higher than in regular precharge, so the noise margins are worse than precharge. Increasing the width of M_E relative to that of the other MOSFETs, by around three times, will reduce the static current. If the width of M_E is further increased, or if the width of M_1 is increased, V_{OL} is reduced and the static current is reduced, this will increase the area that the circuit takes up. When comparing an enhancement load inverter with the hybrid with the same transistor sizes the hybrid has the same V_{OH} but a slightly higher V_{OL}.

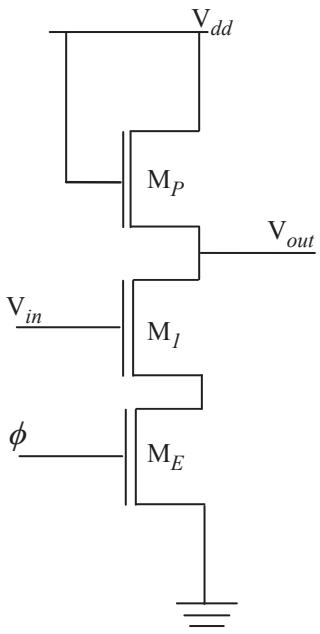


Figure 6.11: Hybrid NMOS Precharge and NMOS Saturated Enhancement Load Inverter.

6.5 Adder Architectures

To investigate the performance of GaAs digital logic with the different logic styles discussed, the sub-components of an 8-bit adder were used as a benchmark for comparison. Adders are essential and reusable IP blocks which are necessary for many key arithmetic functions. There are many different adder architectures with each having it's own advantages. It was decided that speed would be the first priority in design, however this would also be carefully balanced with the associated power consumption and area requirements. In figure 6.12 various adder architectures are compared, it can clearly be seen the the carry-lookahead and the carry-select adders are the most favourable for speed. However there is a relatively little speed advantage by moving to carry-lookahead compared to the extra area incurred. Therefore carry-select was chosen as the architecture to investigate.

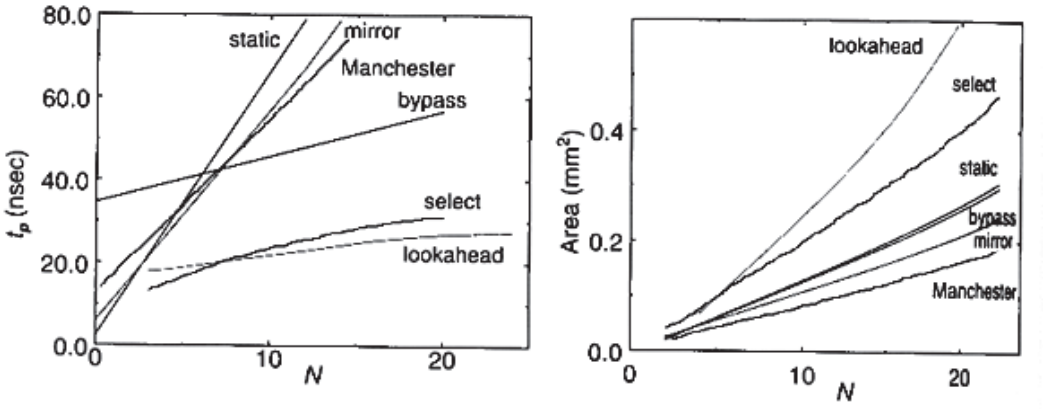


Figure 6.12: Relative Merits of Various Adder Architectures [8].

The architecture of a carry-select adder is shown in figure 6.13. It's speed advantage comes from minimising the carry propagation delay by pre-calculating all of the possible outcomes. Which is why the area is poorer than other alternatives. For each bit pair of inputs An and Bn, the sums (Sn_0, Sn_1) and carry-outs ($C_{out}n_0$, $C_{out}n_1$) are calculated for a carry-in of 0 and 1 simultaneously, using two 1-bit adders. The carry-in (C_{out}n-1) is then used to select the correct result from two 2-input multiplexers. These two sub-components shall be designed and optimised in section 6.6, in some of the different logic styles discussed in section 6.4, in both silicon and GaAs.

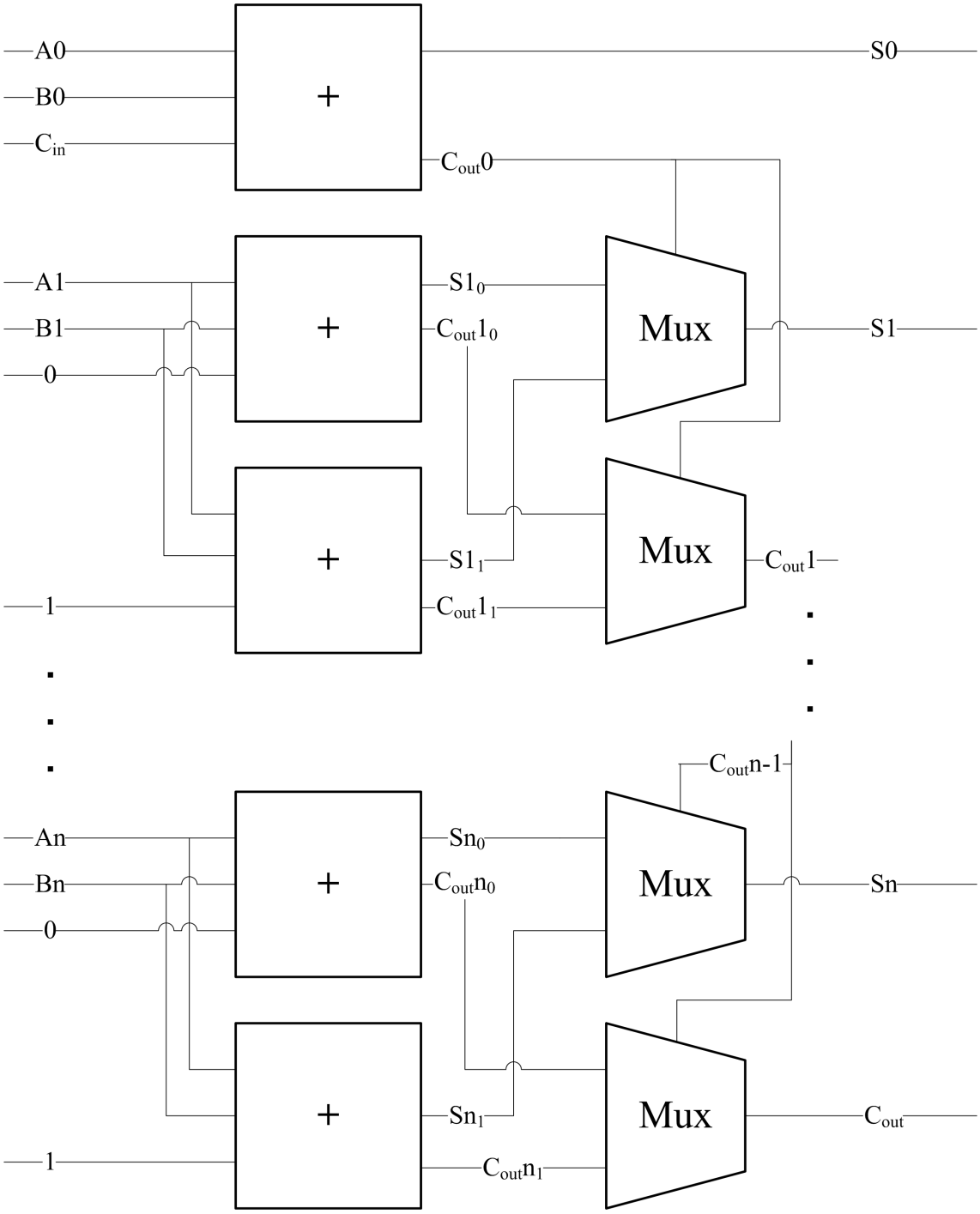


Figure 6.13: Carry Select Adder Architecture.

6.6 Adder Components

The logic styles investigated for the adder sub-components were CMOS, NMOS saturated enhancement load (NMOS) and NMOS precharge logic (precharge). Where an inverter was required on the output in all cases a CMOS inverter was used. This was necessary, especially in the case of the enhancement load NMOS, to restore the logic levels to near full logic swing. For each of the carry-select adder sub-components, in each of the logic styles, the same optimisation methodology was used. This is illustrated in figure 6.14.

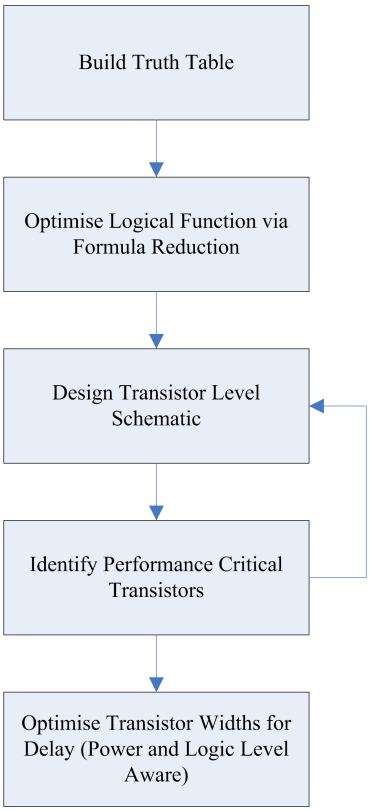


Figure 6.14: Optimisation Process for 8-bit Adder Sub-Components.

6.6.1 1-bit Adder Optimisation

The first step in optimising a logic function is to build it's logic function based on it's truth table. Table 6.1 is the truth table for the 1-bit adder. Equation 6.2

shows the simple (6.2a, 6.2c) and minimised (6.2b, 6.2d) forms of the logic functions that describe this mathematically. By minimising the logic functions we reduce the number of transistors that will be required to create the circuit, before even starting to design the circuit schematic. This can be further minimised by designing at the transistor level rather than the gate level.

As shown in equation 6.2d, $\bar{C_{out}}$ can be used to calculate S, which helps to minimises the number of transistors required. This makes an individual S calculation slightly longer, as the result will not be logically correct until after the delay in calculating $\bar{C_{out}}$. However in a multi-bit adder the propagation delay is a much more significant factor - even when minimised due to choosing an architecture that is sympathetic to this such as carry select. Hence, area can be saved in the S calculation at no overall delay cost.

Table 6.1: Logic States for a 1-bit Adder.

Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$C_{out} = B.C_{in} + A.C_{in} + A.B \tag{6.2a}$$

$$C_{out} = A.B + C_{in}.(A + B) \tag{6.2b}$$

$$S = \bar{A}.\bar{B}.C_{in} + \bar{A}.B.\bar{C_{in}} + A.\bar{B}.\bar{C_{in}} + A.B.C_{in} \tag{6.2c}$$

$$S = A.B.C_{in} + \bar{C_{out}}.(A + B + C_{in}) \tag{6.2d}$$

For each of the logic styles which are presented in the following sections

L = 0.6 μm, W_n = 10 μm, $W_p = W_n$ tSize, and V_{dd} = 3 V. Where the CMOS tSize, W_p/W_n, ratios are 2.5 for silicon and 5 for GaAs. The input test signal was as shown in figure 6.15, which is a 20 MHz signal. The propagation delay times, tphl, tplh, and tp are calculated as the time to propagate the input at $V_{dd}/2$ to the output. The rise and fall times of the output, t_r and t_f, are between 20-80% of V_{dd}.

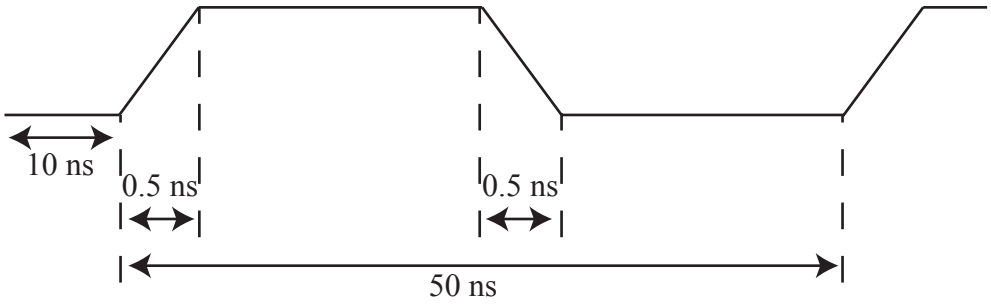


Figure 6.15: Input test signal for timing and power analysis of 1-bit adders and multiplexers.

The energy used per cycle for each function (S and C_{out}) is calculated by integrating the power used over a single clock cycle. The method for this is shown in figure 6.16 and equation 6.3.

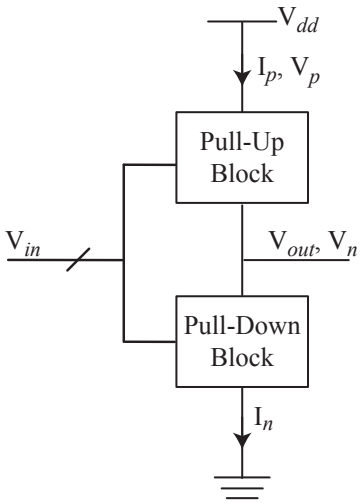


Figure 6.16: General method for calculating power consumption.

$$\begin{aligned} P_p &= |I_p V_p| \\ P_n &= |I_n V_n| \\ P_i &= P_p + P_n \\ E &= \int P_i \; dt \end{aligned} \tag{6.3}$$

The speed and power results for the logic styles investigated, CMOS, NMOS saturation enhancement load (NMOS) and NMOS precharge (precharge), are summerised in section 6.6.1.4.

6.6.1.1 CMOS

First the CMOS version of the circuit was developed as a benchmark, equations 6.2b and 6.2d were used to design the circuit. In a compound gate like this further transistor sizing (beyond the W_p/W_n ratio) is required to compensate for the differences in the stack depths in the circuit. The stack depth is the number of transistors that are connected in series - each pull-up and pull-down path will have an associated stack depth. There are established methods for sizing CMOS circuits, the *linear deepest stack first* method was used in this case [8]. Figure 6.17 shows the circuit schematic with the associated transistor widths. The speed and power results and area estimates are shown in section 6.6.1.4.

6.6.1.2 NMOS Saturated Enhancement Load

As discussed in section 6.4.2 NMOS saturated enhancement load circuits can be design using only NMOS circuits. The pull down part of the circuit is designed and sized like CMOS, however the pull up PMOS network is replaced by a single NMOS device. The circuit diagram for the NMOS circuit is shown in figure 6.18, which is based on equations 6.2b and 6.2d. It can be seen that where an invert function was required a CMOS inverter was used. Using the CMOS inverter helps to restore the logic levels to *full swing* for this style.

As mentioned in section 6.4.2 the static characteristics did not gain much from adjusting the strength of the pull up in the NMOS circuits, however this was inves-

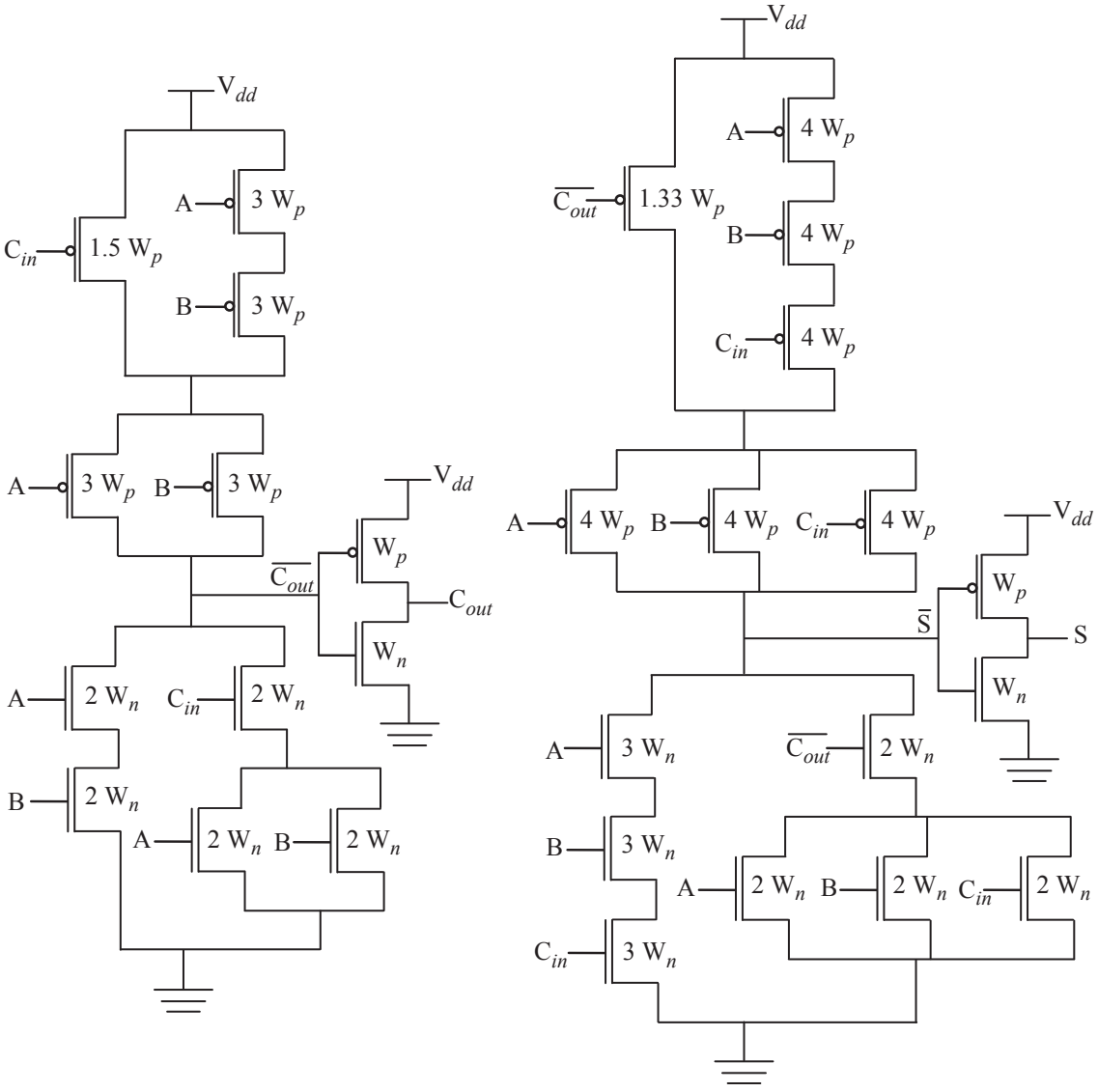


Figure 6.17: CMOS 1-bit adder schematic showing relative device widths. L = 0.6 μm, W_n = 10 μm, and W_p = W_n tSize, where tSize is 2.5 for silicon and 5 for GaAs.

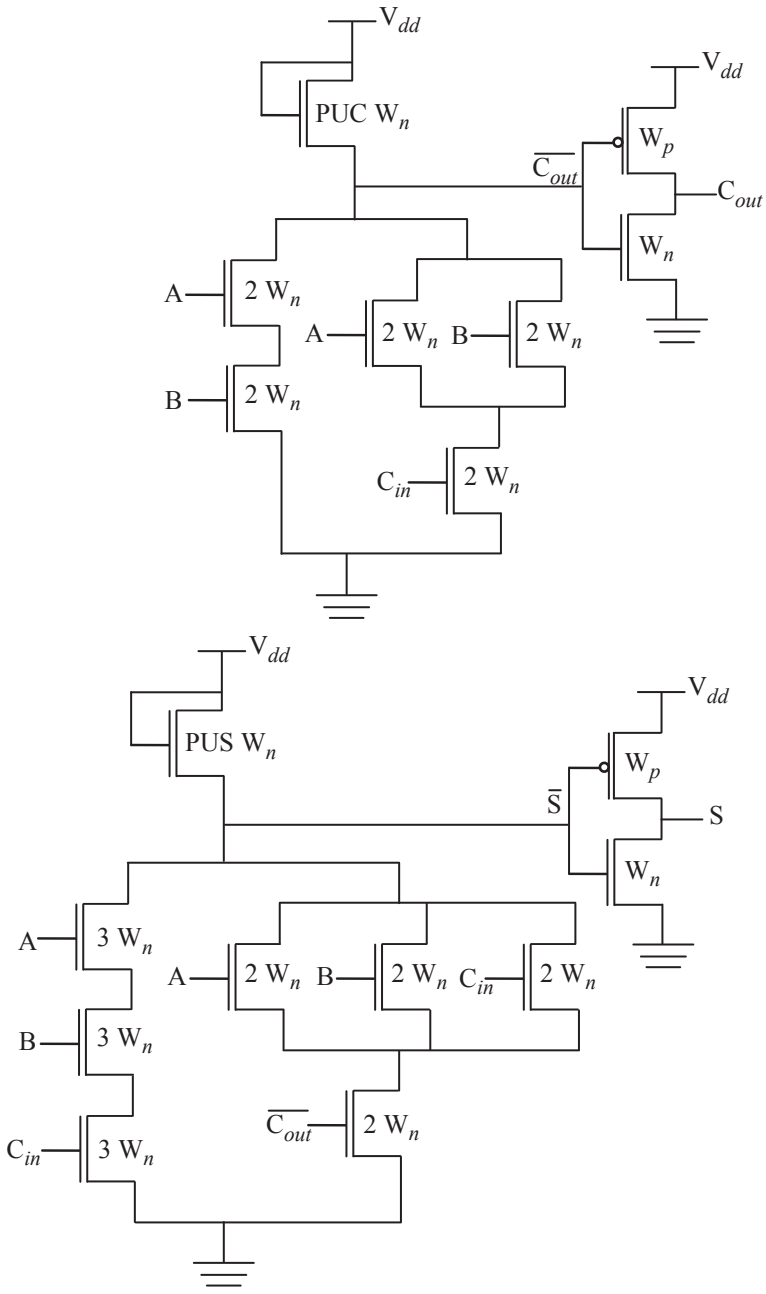


Figure 6.18: NMOS 1-bit adder schematic showing device width parameters. L = 0.6 μm, W_n = 10 μm, and W_p = W_n tSize, where tSize is 2.5 for silicon and 5 for GaAs.

tigated with reference to timing. To optimise the design the widths of the pull up devices (pull up for C, PUC, and pull up for S, PUS) were swept from 1 to 10 to see if any minima could be identified in the average delay ((tphl(S) + tplh (S) + tphl(C_{out}) + tplh(C_{out}))/4). Where any minima was identified this was used to fix the size of the transistor.

All sizing decisions also took into account the effects on the power consumption and the logic swing. Logic swing was important particularly for this style as it is difficult to achieve full rail-to-rail swing. At $V_{dd} = 3$ V, typically a logic swing of ≥ 2.9 V was achieved for the NMOS style. Where the speed decreased but with no clear minima, any power consumption minima were used to identify the best choice of transistor size.

It was found that for both silicon and GaAs the optimum sizings were, PUC = 4 and PUS = 3. The speed and power results and area estimates are shown in section 6.6.1.4.

6.6.1.3 NMOS Precharge

For the precharge style it was found that due to the timing constrains of the clock that it was necessary to use the forms of S and C_{out} as in equations 6.2b and 6.2c. Therefore S is no longer waiting for the result of C_{out} but is being calculated concurrently.

As discussed in section 6.4.2 NMOS precharge circuits are designed using an NMOS pull down network like CMOS with the addition of a clocked NMOS transistor next to the ground connection. The PMOS pull up network is replaced with a single clocked PMOS transistor.

The circuit diagram for the precharge circuit is shown in figure 6.19. It can be seen that where an invert function was required a CMOS inverter was used. Using the CMOS inverter in this case is more efficient in terms of the number of transistors used, as the precharge inverter requires 2 NMOS and 1 PMOS transistors.

The pull down network was sized as CMOS. In this case the width multipliers PUC and PUS were again optimised. As in section 6.6.1.2 each of these width multipliers was swept from 1 to 10 to see if any minima could be identified in the average delay, taking into account the effects on the power consumption and

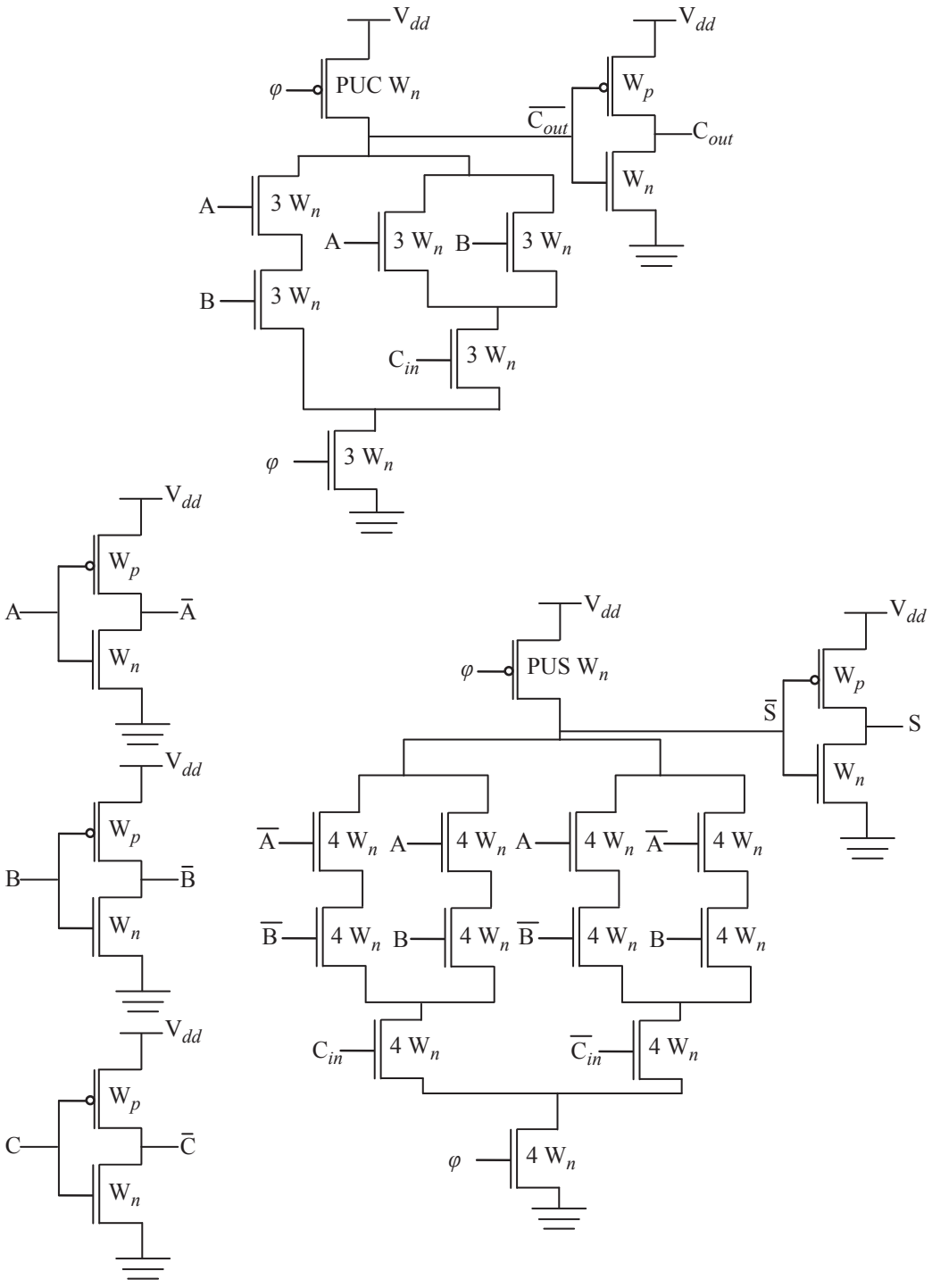


Figure 6.19: Precharge 1-bit adder schematic showing device width parameters. L = 0.6 μm, W_n = 10 μm, and W_p = W_n tSize, where tSize is 2.5 for silicon and 5 for GaAs.

the logic swing. Where the speed decreased but with no clear minima, any power consumption minima were used to identify the best choice of transistor size.

It was found that for for silicon the optimum sizings were, PUC = PUS = 4 and for GaAs PUC = PUS = 3. The speed and power results and area estimates are shown in section 6.6.1.4. The speed and power results and area estimates are shown in section 6.6.1.4.

6.6.1.4 Comparison

The results for the optimised designs in sections 6.6.1.1, 6.6.1.2, and 6.6.1.3 are shown below in tables 6.2, 6.3, and 6.4. It can be seen that the minimised average propagation delays (and rise and fall times) are larger for the GaAs circuits. As discussed in section 6.3 this is due the higher access resistance in the GaAs devices and may also be due to the fact that the higher electron velocity in GaAs will only be observed in shorter channel devices. As this data becomes available these methods can be used to see if any improvement can be observed in manufactured short channel GaAs devices.

To gain a clearer understanding of the above results the average delay and total energy used for each style in silicon and GaAs are normalised to the values for CMOS in the particular material. It can be seen from tables 6.5 and 6.6 that the GaAs circuits gain a similar speed up advantage to silicon, by moving to non-CMOS circuit styles. However, for both of the alternative styles, NMOS and precharge, GaAs gains more in power and area compared to silicon. The area estimates are based on the number of devices in each circuit, and the lengths, widths and scaling factors used.

For both silicon and GaAs, NMOS is the best style for speed and area, and precharge for power consumption. Using the NMOS style approximately halves the speed, however the cost in power may be prohibitive depending on the system requirements.

The precharge style not only yields the best performance in terms of power but also gives an improvement in speed (20-25 %) and area (25-35 %) . The GaAs circuits gain more comparitave advantage ($\approx$ 10 %) in both power and area to silicon when using this design style. Precharge may therefore may be the most appropriate when designing with GaAs MOSFETs.

Table 6.2: 1-bit Adder Speed and Power Results for Sum (S).

Circuit Style	Material	tphl (ps)	tplh (ps)	Average Delay (ps)	t_r (ps)	t_f (ps)	Energy (pJ)
CMOS	Si	396.00	356.10	376.05	58.46	84.65	17.37
CMOS	GaAs	668.60	1005.00	836.80	203.90	221.40	69.42
NMOS	Si	188.70	197.00	192.85	148.70	120.40	415.40
NMOS	GaAs	552.30	387.40	469.85	241.50	405.60	613.40
Precharge	Si	175.00	359.30	267.15	66.56	35.90	12.36
Precharge	GaAs	443.70	826.10	634.90	188.00	117.90	39.77

Table 6.3: 1-bit Adder Speed and Power Results for Carry (C_{out}).

Circuit Style	Material	tphl (ps)	tplh (ps)	Average Delay (ps)	t_r (ps)	t_f (ps)	Energy (pJ)
CMOS	Si	323.40	259.10	291.25	50.35	46.41	22.84
CMOS	GaAs	532.40	535.90	534.15	140.00	143.80	71.49
NMOS	Si	119.40	165.80	142.60	95.37	95.31	724.10
NMOS	GaAs	427.80	293.50	360.65	184.70	330.00	1130.00
Precharge	Si	174.00	291.00	232.50	62.88	34.01	14.18
Precharge	GaAs	410.60	561.20	485.90	155.20	98.50	36.28

Table 6.4: Average 1-bit Adder Speed and Power Results.

Circuit Style	Material	Average Delay (ps)	Average t_r (ps)	Average t_f (ps)	Total Energy (pJ)
CMOS	Si	333.65	54.41	65.53	40.21
CMOS	GaAs	685.48	171.95	182.60	140.91
NMOS	Si	167.73	122.04	107.86	1139.50
NMOS	GaAs	415.25	213.10	367.80	1743.40
Precharge	Si	249.83	64.72	34.96	26.54
Precharge	GaAs	560.40	171.60	108.20	76.05

In fact, this is the worst case propagation delay for precharge logic. If we consider a combination of inputs during the precharge phase, that result in a logically high output, then there will be effectively no propagation delay [84], except for that through the CMOS inverter on the output. Therefore, it is expected that the speed of the precharge circuits would on average perform better than this worst case.

Table 6.5: Silicon 1-bit Adder Results Normalised to CMOS.

	Average Delay	Total Energy Used Per Cycle	Area
CMOS	1.00	1.00	1.00
NMOS	0.5	28.34	0.31
Precharge	0.75	0.66	0.76

Table 6.6: GaAs 1-bit Adder Results Normalised to CMOS.

	Average Delay	Total Energy Used Per Cycle	Area
CMOS	1.00	1.00	1.00
NMOS	0.61	12.37	0.20
Precharge	0.82	0.54	0.66

6.6.2 Multiplexer Optimisation

The multiplexer is treated the same way as the 1-bit adder in section 6.6.1. The truth table is shown in table 6.7 and the logic function is as shown in equation 6.4. As previously L = 0.6 μm, W_n = 10 μm, W_p = W_n tSize, and V_{dd} = 3, and tSize (W_p/W_n) is 2.5 for silicon and 5 for GaAs. The input signal is as in figure 6.15.

Table 6.7: Logic States for a 2-input Multiplexer.

Inputs			Outputs
A0	A1	S	A
0	0	0	0 (A0)
0	0	1	0 (A1)
0	1	0	0 (A0)
0	1	1	1 (A1)
1	0	0	1 (A0)
1	0	1	0 (A1)
1	1	0	1 (A0)
1	1	1	1 (A1)

$$A = S.A1 + \bar{S}.A0 \tag{6.4}$$

6.6.2.1 CMOS

The CMOS version of the circuit is as shown in figure 6.20. The linear deepest stack first method was again used to appropriately size the transistors. The speed and power results and area estimates are shown in section 6.6.2.4.

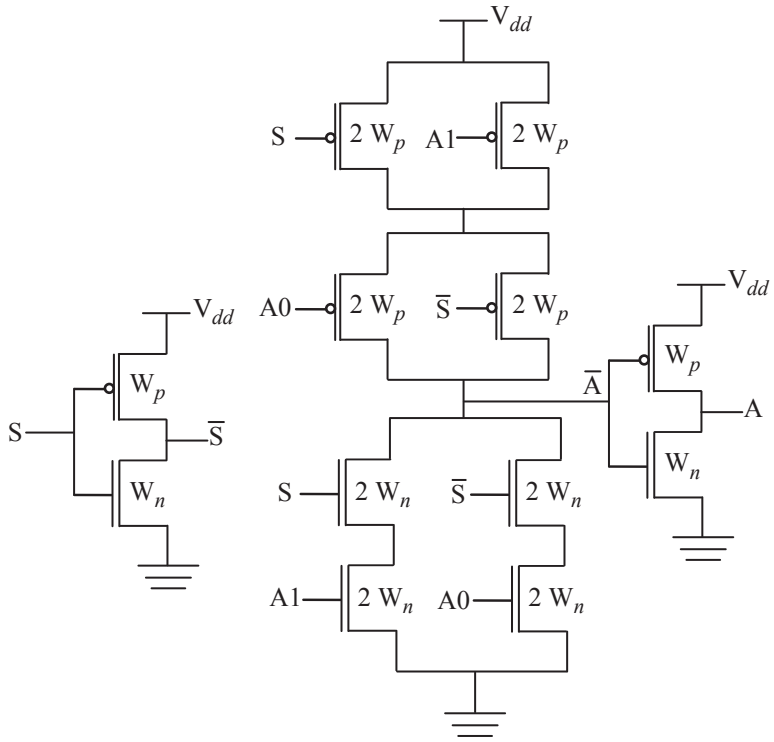


Figure 6.20: CMOS multiplexer schematic showing relative device widths. L = 0.6 μm, W_n = 10 μm, and W_p = W_n tSize, where tSize is 2.5 for silicon and 5 for GaAs.

6.6.2.2 NMOS Saturated Enhancement Load

The NMOS version of the multiplexer is shown in figure 6.21. The method used to optimise the circuit was as in section 6.6.1.2. In this case the width multiplier that was optimised was PU, as shown in figure 6.21. The resulting optimum widths were PU = 2 for silicon, and PU = 4 for GaAs. The speed and power results and area estimates are shown in section 6.6.2.4.

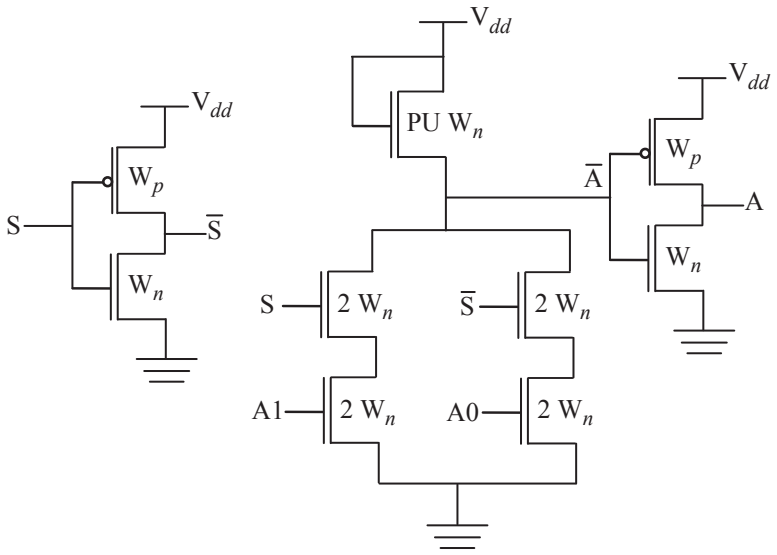


Figure 6.21: NMOS multiplexer schematic showing device width parameters. L = 0.6 μm, W_n = 10 μm, and W_p = W_n tSize, where tSize is 2.5 for silicon and 5 for GaAs.

6.6.2.3 NMOS Precharge

The precharge version of the multiplexer is shown in figure 6.22. The method used to optimise the circuit was as in section 6.6.1.2. In this case the width multiplier that was optimised was again PU, as shown in figure 6.22. The resulting optimum widths were PU = 4 for silicon, and PU = 4 for GaAs. The speed and power results and area estimates are shown in section 6.6.2.4.

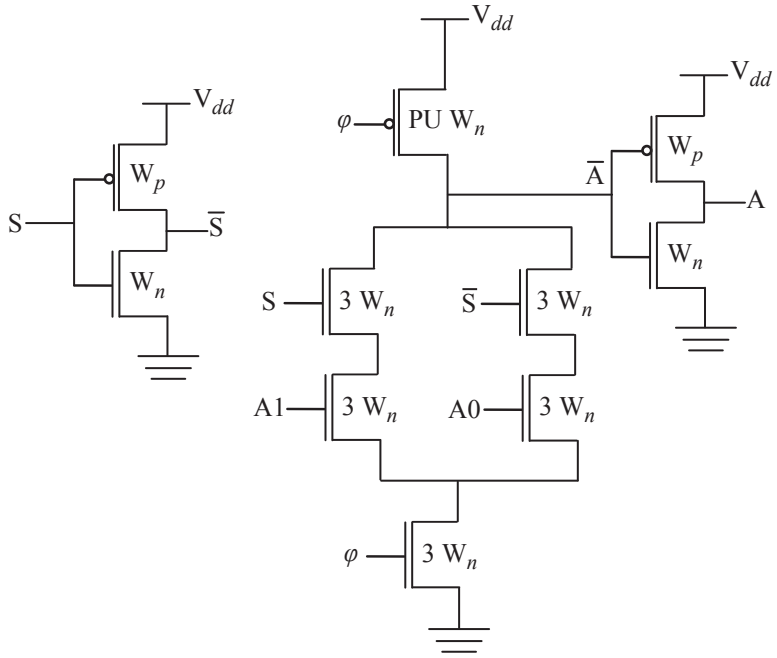


Figure 6.22: Precharge multiplexer schematic showing device width parameters. L = 0.6 μm, W_n = 10 μm, and W_p = W_n tSize, where tSize is 2.5 for silicon and 5 for GaAs.

6.6.2.4 Comparison

The results from sections 6.6.2.1, 6.6.2.2, and 6.6.2.3 are shown below in table 6.8. As with the 1 bit adders, it can be seen that the minimised average propagation delays (and rise and fall times) are larger for the GaAs circuits. As discussed previously this is mainly due the higher access resistance in the GaAs devices.

The normalised average delay and total energy for each style in each technology is shown for the multiplexers in tables 6.9 and 6.10. For both silicon and GaAs, NMOS is the best style for speed and area, and precharge for power consumption. Using the NMOS style approximately halves the speed, however the cost in power may be prohibitive depending on the system requirements. In this case, GaAs gains more by moving to non-CMOS circuit styles, in speed, power and area, compared to silicon. The area estimates are based on the number of devices in each circuit, and the lengths, widths and scaling factors used.

There are clearly trade-offs to be made between speed, power, and area. For GaAs the precharge style not only yields the best performance in terms of power but also gives significant improvements in speed (26 %) and area (48 %). It can be seen that in this case there is no speed up advantage for silicon moving to precharge.

Table 6.8: Multiplexer Speed and Power Results.

Circuit Style	Material	tphl (ps)	tplh (ps)	Average Delay (ps)	t_r (ps)	t_f (ps)	Total Energy (pJ)
CMOS	Si	262.20	198.00	230.10	69.06	44.86	9.98
CMOS	GaAs	685.80	813.80	749.80	206.00	132.30	42.15
NMOS	Si	127.40	156.70	142.05	107.90	133.80	343.70
NMOS	GaAs	428.10	395.40	411.75	300.20	448.30	639.20
Precharge	Si	219.60	267.10	243.35	56.11	40.79	6.18
Precharge	GaAs	622.70	483.20	552.95	141.40	126.30	17.25

Table 6.9: Silicon 2-Input Multiplexer Results Normalised to CMOS.

	Average Delay	Total Energy Used Per Cycle	Area
CMOS	1.00	1.00	1.00
NMOS	0.62	34.46	0.49
Precharge	1.06	0.62	0.74

Table 6.10: GaAs 2-Input Multiplexer Results Normalised to CMOS.

	Average Delay	Total Energy Used Per Cycle	Area
CMOS	1.00	1.00	1.00
NMOS	0.55	15.16	0.40
Precharge	0.74	0.41	0.52

6.7 Summary

The compact models developed in chapter 5 have been used to investigate the potential performance of GaAs digital logic. The models were imported in to standard design tools to facilitate this comparison. CMOS was first investigated and it was found that the static characteristics of the GaAs circuits were superior to silicon, however silicon performed better in the transient analysis.

The sub-components of a carry-select adder (1 bit adder and 2 input multiplexer) were used to analyse the differences in performance between silicon and GaAs in various circuit styles. CMOS, NMOS saturated enhancement load, and NMOS precharge were used for this. Each circuit in each style was carefully optimised to achieve the best possible results for each of the technologies explored.

Although the speed and power in the GaAs designs was worse than silicon this may be explained due to the following factors. Principally the lower performance can be attributed to the higher access resistance in the GaAs devices. The contact and sheet resistance of the devices investigated is high compared to the silicon devices used in the comparison. They are also high compared to the most recent developments for GaAs devices [44, 85]. Secondly, as explained earlier is that GaAs's true potential for digital logic may only be seen at smaller gate lengths where the ballis-

tic and overshoot effects dominate. Finally, GaAs has a lower thermal conductivity than silicon which may also play a part.

GaAs gains a larger comparative advantage when moving to non-CMOS circuit styles than silicon. This is due to the poor performance of the PMOS devices being minimised by use of alternative pull-up networks. Although the NMOS saturated enhancement load is the best in terms of speed and area, it's power requirements may be prohibitive. The NMOS precharge style gains in speed, power, and area compared to CMOS for both silicon and GaAs, however the relative merits are much more apparent in the GaAs circuits. Therefore, NMOS precharge logic is recommended as the design style to be used for GaAs digital logic. Dynamic logic styles such as precharge can be more challenging to design with, however they are being increasingly used in designs where there are extremely performance critical areas [83].

7 Conclusion

7.1 Thesis Summary

This thesis has provided an investigation into the potential performance of GaAs MOSFETs for digital logic. This has been achieved by first developing models, both physical and compact, of GaAs/Ga_2O_3 devices. The compact models then enabled circuit simulations with the GaAs devices. Hence, finally, an investigation into appropriate digital design style for this technology could be completed. The devices used for this investigation were 0.6 μm gate length, enhancement mode, GaAs heterostructure MOSFETs, with a high-κ dielectric (Ga_2O_3), and an InGaAs channel.

2D drift-diffusion models were developed based on measured device characteristics, physical material properties, and MOSFET theory. These models were carefully calibrated to the available data to ensure that accurate device parameters could be derived for the next stage: compact modelling. The compact models were created by adapting industry standard BSIM3v3.2 Si/SiO_2 compact models for use with the GaAs/Ga_2O_3 device structure. These were developed using the available device data and the results from the drift-diffusion simulations. Additionally, a method called ratio correction was used to indirectly access internal BSIM model parameters to ensure that the correct physical constants were used in calculations. Both physical

and compact models demonstrate well matched characteristics to the data.

Potential digital design styles for GaAs have been discussed, simulated, and compared. As a further comparison, the same circuits have been simulated in an established silicon technology at the same technology node. The results indicate that the GaAs devices can be used to build correctly functioning digital circuits in several different design styles. The static characteristics, including the noise margins, are better for the GaAs logic gates. However, at this technology node, and with this particular GaAs MOSFET device design, the speed of GaAs logic gates does not outperform that of similarly sized silicon devices.

As a consequence of the poor performance of GaAs PMOS devices, GaAs digital logic gains a larger comparative advantage by designing in non-CMOS circuit styles than silicon. This is due to the use of alternative pull-up networks that utilise less PMOS devices. It is clear that trade-offs must be made when choosing a design style for GaAs digital circuits, and although the NMOS saturated enhancement load is the best in terms of speed and area, it's power requirements may be prohibitive. The NMOS precharge style has advantages in both speed, power and area compared to CMOS, and as a consequence is recommended for designing GaAs digital logic.

Throughout, reference has been made to current research and technical developments, along with the underlying theory to explain the methods used and results observed. The project motivation has been explained in the context of technological developments, and in the context of the semiconductor industry. It is critical to understand not only the technology but why and how it might be of relevance to the industry, and why it might be considered to have a competitive advantage to existing technologies. Additionally, some of the core business and management issues that were studied were discussed, along with illustrative examples to demonstrate their relevance to real-life work situations.

7.2 Conclusions

This work demonstrates the first circuit design methodology investigation with GaAs MOS technology, using industry standard circuit design tools, and GaAs adapted compact MOSFET models. It shows that, as expected, traditional CMOS circuit design will not be the most appropriate circuit design style for this technology, and

design recommendations have been made.

To enable this circuit investigation, novel GaAs compact model have been developed by adapting existing industry standard models for silicon CMOS. These compact models include some necessary approximations using effective medium theory and simplified mobility models. Additionally, further adjustments, or ratio corrections, were introduced to ensure that the internal physical parameters were correct. This was due to the limitations of the compact models that were available at the time. The models have been shown to have characteristics that are well matched to data from real GaAs PMOS devices, and with drift-diffusion models of GaAs PMOS and NMOS devices.

The drift-diffusion models were created and calibrated to available device data. This modelling was required to investigate the physical parameter values, such as doping, and gate work function, that were not given with the data, and were necessary to construct the compact models.

This investigation has shown that GaAs MOS could be used as a viable technology for digital circuits as long as appropriate design styles are considered. The performance of the circuits is likely to have been limited by the less than ideal characteristics of the device data. At this gate length it it likely that the velocity saturation is dominating the characteristics, not the mobility. The velocity saturation of the channel material, InGaAs, is equivalent to that of silicon, and the velocity saturation of GaAs is lower than silicon. Furthermore, it is likely that the true potential for GaAs MOSFET digital logic may only be seen at smaller gate lengths where the ballistic and overshoot effects will dominate. Most significantly, the device parasitics may be limiting the performance. The contact and sheet resistance of the devices investigated is high compared to the silicon devices used for comparison, and to recent developments for GaAs devices [44, 85]. Since this work was started device characteristics for GaAs devices have continued to improve, as a consequence, the methodology in this work could be reused to develop models of new, higher performance, devices in the future.

Over the last 20 years, GaAs MOSFETs for digital design have had occasional leaps forward in development, and a wealth of press articles citing this as the next big thing have always followed. Device development is finally beginning to reach a level of maturity that means it can be seriously considered as a future enabling

technology.

The key issue when introducing new technologies is that silicon has so far been reliable, scaled well, and its manufacturing processes are well understood. Therefore, it is critical that companies and designers are able to see significant added value in moving to a new technology, especially if there are added design challenges, or increased costs. If they are able to envisage achieving a competitive advantage through this, then it is likely that some will make the move. However, this will not be without risk. Further development is required to push GaAs MOSFETs forward as a viable competitive alternative to silicon digital circuits. Device development to improve characteristics is ongoing, and this will be the key to it's successful introduction in to the digital market. Moreover, if a fully integrated digital, RF, and optoelectronic platform can be offered by GaAs then it will certainly find a place in the market.

As silicon scaling starts to reach its limits, technologists and designers will need to become more open minded about potential new technologies, and the issues associated with designing circuits with deconanometer gate length devices. Device variability is starting to dominate the characteristics of silicon devices at gate lengths < 45 nm. Therefore, more than ever before, research into devices that provide a viable alternative to silicon with improvements in either integration or performance will be favourably considered in the main stream. The ITRS now places diversification highly along with miniturisation, and a combination of these will be necessary if the semiconductor industry is to continue to follow it's previous successes and continue to achieve Moore's law.

Silicon production and economies of scale are well established, therefore it is important that new technologies provide easy integration with these processes, or provide significant advantages as a stand-alone new technology and process. The potential to have GaAs devices on a silicon substrate offers interesting possibilities. GaAs provides significant improvements in the characteristics for NMOS devices, however the PMOS performance is poor. Conversely to GaAs, germanium PMOS devices perform better than silicon. However, so far NMOS devices have not been demonstrated that significantly outperform silicon [86]. Germanium can also be grown on silicon, and devices have been demonstrated on a silicon substrate [86–88]. This includes high performance devices that are compatible with a silicon process

flow. Additionally, it has been shown that GaAs can be grown on germanium [69, 89]. So perhaps we may eventually be able to integrate these complimentary high performance devices along side silicon CMOS.

7.3 Future Work

Future work in this area includes further improvements in device characteristics, and the production of smaller gate length devices. It is clear that progress is being made in this direction for GaAs NMOS devices with characteristics making steady improvements, and gate lengths of devices being further scaled to 0.3 μm. Additionally, Monte Carlo modelling of devices with gate lengths $\leq$ 100 nm show optimistic results for the future. Subsequent compact model development and circuit design investigations would certainly take into account these device improvements.

Improvements in the characteristics of PMOS devices is particularly pertinent to digital circuit design, however currently GaAs PMOS device performance is poor compared to the NMOS devices. As shown in this work, it is possible to minimise the use of PMOS devices in circuit designs and see improvements in the performance for this technology. However, eliminating PMOS devices entirely from designs leads to performance trade-offs that many designers would find unacceptable. As a consequence, it is important that the characteristics of GaAs PMOS devices are improved, or we must consider how high performance GaAs NMOS devices can be integrated with an alternative PMOS technology. There are two possibilities for this; either silicon PMOS devices could be used with the GaAs NMOS devices using GaAs-on-Si technology, or as discussed previously future possibilities may lie in the integration of germanium and GaAs on silicon a substrate (using either GaAs-on-Si or GaAs-on-Ge, and Ge-on-Si technology).

Recent developments in the BSIM4 model may change how future GaAs compact models are developed. The latest release of BSIM4 includes a new material model for the predictive modeling of non-SiO_2 gate dielectrics, non-poly silicon gates and non-silicon channels [90, 91]. This means that some of the ratio corrections discussed in this work would not be necessary in the next generation of GaAs MOSFET compact models. However, the correct calculation of the GaAs parameters would still be necessary, along with knowledge of the correct physical parameters, either

from process knowledge or from modelling. It may still be necessary to include the use of effective medium theory where complex heterostructures are used in devices.

These developments in devices and models could be integrated with the methodology in this thesis to revisit GaAs digital logic design in the future.

Appendix A
Motorola MRC6011 Fact Sheet

Fact Sheet

MRC6011

RECONFIGURABLE COMPUTE FABRIC (RCF) DEVICE

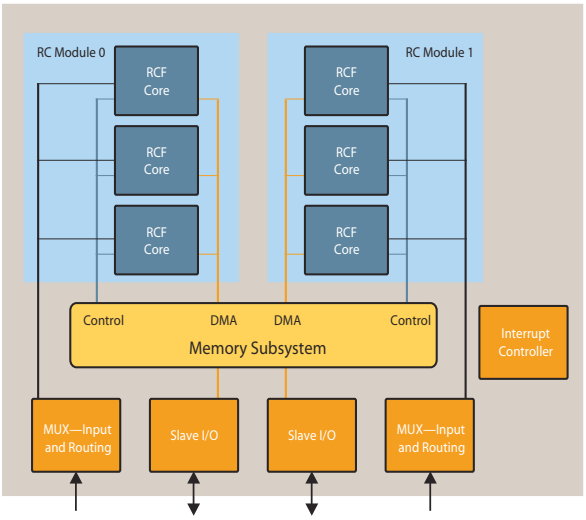
MOTOROLA intelligence everywhere | digital dna

Ushering in a new era in signal processing, the 24 Giga MACS MRC6011 is Motorola's first Reconfigurable Compute Fabric (RCF) device. Ideally suited for MIPS-intensive, repetitive tasks, the MRC6011 offers a resource-efficient solution for computationally intensive applications, such as baseband processing for 2.5G and 3G basestations; broadband wireless access systems; and signal processing for advanced features such as Adaptive Antenna (AA) and Multi-User Detection (MUD). The highly programmable MRC6011 device offers system-level flexibility and scalability while inducing competitive cost and power consumption metrics.

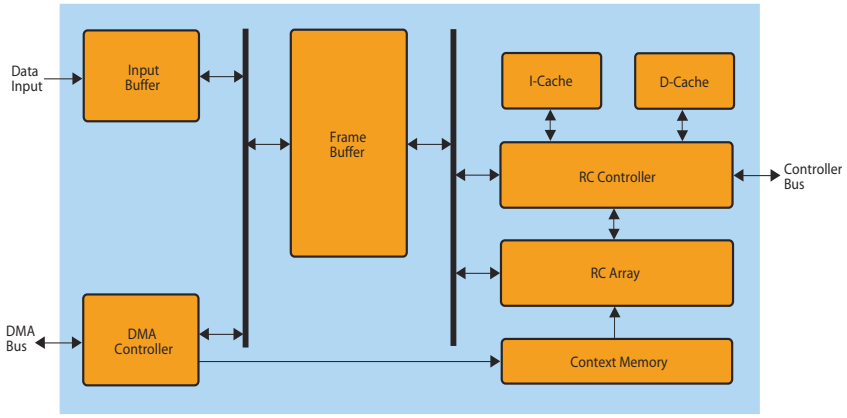
The MRC6011 consists of six RCF cores, an optimized memory subsystem and specialized external interfaces. Each RCF core consists of an array of 16 reconfigurable cells (RCs) connected through an extremely flexible and high-bandwidth fabric. The core also features high-speed local buffers and a RISC processor.

The MRC6011 device complements traditional DSPs in an efficient system-level solution: The MRC6011 is designed to process MIPS-intensive, repetitive tasks and a DSP, such as the MSC8126, performs higher complexity, irregular tasks. The C and assembly programmability of the MRC6011 helps ensure flexibility, ease of programming and integrated tools at the system level, which can result in low total cost of ownership for equipment manufacturers.

THE MRC6011 DEVICE OFFERS THE BENEFITS OF A PROGRAMMABLE DSP SOLUTION FOR BASEBAND PROCESSING, WHILE ZEROING IN ON THE COST, POWER CONSUMPTION AND PROCESSING CAPABILITY OF A TRADITIONAL ASIC-BASED APPROACH.



MRC6011 BLOCK DIAGRAM



RCF CORE BLOCK DIAGRAM

FEATURES

RCF Core-Level Features

- Optimized RISC processor for efficient C code compilation
  - Instruction and data cache
- RC array of 16 RC cells, each featuring:
  - Pipelined MAC unit
  - Arithmetic, logical and conditional units
  - Special-purpose complex correlation unit
- Large I/O buffers
- Single and burst transfer DMA controller

Device-Level Features

- Six RCF cores in two modules of three cores
- Two multiplexed data input (MDI) interfaces
- Two slave I/O bus interfaces
- Host visible memory for control code and for traffic sharing
- Inter-module DMA-based data sharing
- Single clock input and JTAG support
- 0.13µ process technology
- Internal logic voltage of 1.2V and I/O voltage of 3.3V
- 31 mm x 31 mm Tape Ball Grid Array (TBGA) package
- Under 3W typical power consumption

BENEFITS

- Up to 24 Giga 16-bit MACS of processing power at 250 MHz
- Up to 48 Giga 4-bit complex correlations per second at 250 MHz
- High throughput and specialized interfaces for basestation applications
- Programmability in C and assembly ensures:
  - Field-upgradability
  - Flexibility to support multiple standards
  - Flexibility to add advanced features later
- Scalable architecture
- Glueless connectivity to industry standard DSPs
- Software tools and application modules
  - Metrowerks' award-winning Integrated Development Environment (IDE)
  - Real-time debug capability for each RCF core
- Library of functions and modules for 3G baseband and other applications

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MOTOROLA

MRC6011FS/D
REV 0

Appendix B
Medici Device Code for GaAs PMOS

```
$ A simulation of the Motorola pmos GaAs device (26th) 4 May 2005
$ Sonia Paluchowski EngD Research Engineer
$ 22-10 used as a start

$ Specify a rectangular mesh**********************************

$ All distances in microns (WIDTH, DEPTH, L, H1, Y.MIN)

MESH SMOOTH=1
X.MESH WIDTH=4 H1=0.1

$ Mesh for the oxide
Y.MESH N=1 L=-0.009
Y.MESH N=10 L=0

$ Mesh varying with depth below oxide
Y.MESH DEPTH=0.002 H1=0.0001
Y.MESH DEPTH=0.031 H1=0.0005
Y.MESH DEPTH=0.003 H1=0.0001
Y.MESH DEPTH=0.004 H1=0.0005
Y.MESH DEPTH=0.050 H1=0.001
Y.MESH DEPTH=0.510 H1=0.01
Y.MESH DEPTH=0.400 H1=0.1
Y.MESH DEPTH=1 H1=0.5
```

```
$ Eliminate some unecessary mesh points
ELIMIN COLUMNS Y.MIN=1

$*************************************************************

$ Specify oxide, GaAs, AlGaAs and InGaAs regions***************
$ All distances in microns (Y.MIN, Y.MAX)

$ Structure as in paper
$ If 2ML = 0.5nm
REGION NAME=GA2O3 INSULATO Y.MAX=0
REGION NAME=GAASML GAAS Y.MIN=0 Y.MAX=0.0005
REGION NAME=ALGAAS ALGAAS Y.MIN=0.0005 Y.MAX=0.0155
+ X.MOLE=0.75
REGION NAME=INGAAS INGAAS Y.MIN=0.0155 Y.MAX=0.0305
+X.MOLE=0.2
REGION NAME=GAAS GAAS Y.MIN=0.0305

$*************************************************************

$ Electrode definition*****************************************
$ All distances in microns (X.MIN, X.MAX)

$ Gate and substrate as paper
ELECTR NAME=Gate X.MIN=1.7 X.MAX=2.3 TOP
ELECTR NAME=Substrate BOTTOM

$ Source and drain width not given so sensible value chosen
ELECTR NAME=Source X.MAX=0.5 Y.MAX=0
ELECTR NAME=Drain X.MIN=3.5 Y.MAX=0

$*************************************************************

$ Specify the doping throughout the device*********************
```

```
$ Doping quantities in cm-3 (N.PEAK)
$ All distances in microns (X.MIN, WIDTH, Y.MIN, Y.CHAR, Y.JUNC)

$ Specify substrate impurity-must be greater than GaAs ni=2.25e6
PROFILE N-TYPE N.PEAK=8E16 UNIFORM OUT.FILE=MDGAAS1DS

$ Delta Doping given in paper as 3.3e11 cm-2
$ => 3.3e11 cm-2 * 1e7 (1/1nm) cm-1 = 3.3e18 cm-3
$ If 2ML = 0.5nm
PROFILE N-TYPE UNIFORM Y.MIN=0.0335 DEPTH=0.001 N.PEAK=3.3e18

$ Specify Source and Drain Doping
$ 5e19 is the limit for S/D doping in GaAs
PROFILE P-TYPE N.PEAK=2.125E19 X.MIN=0.0 WIDTH=1.6
+ X.CHAR=0.01 Y.MIN=0 DEPTH=0.2 Y.CHAR=0.01
PROFILE P-TYPE N.PEAK=2.125E19 X.MIN=2.4 WIDTH=1.6
+ X.CHAR=0.01 Y.MIN=0 DEPTH=0.2 Y.CHAR=0.01

$***************************************************************

$ Interface Trap Density
$ Trapped charge density for the electron acceptors in cm-2/eV
$(N.ACCEPT)
$INTERFACE REGION=(GA2O3,GAASML) N.ACCEPT=3E11

$ Plot the mesh
PLOT.2D GRID TITLE="pmos GaAs - Grid" FILL SCALE PLOT.OUT="Grid"

$***************************************************************

$ Defining Ga2O3 Material Properties*****************************
$ Energy bandgap at 300K in eV (EG300)
$ Density in Kg/cm3 (DENSITY)

MATERIAL REGION=GA2O3 PERMITTI=10 EG300=4.9 DENSITY=0.006
```

```
$*************************************************************

$Define permittivities*****************************************

MATERIAL REGION=ALGAAS PERMITTI=10.7
MATERIAL REGION=INGAAS PERMITTI=13.15

$*************************************************************

$ Specify contact parameters***********************************
$ Workfunction of materials in V (WORKFUNC)
$ Resistance in Ohm-um (RESISTAN)

CONTACT NAME=Gate WORKFUNC=4.68

$ From paper - Contact resistance(1050)
$ + sheet resistance(1480.8) = 2530.8

CONTACT NAME=Source RESISTAN=2530.8
CONTACT NAME=Drain RESISTAN=2530.8

$*************************************************************

$ Specify physical models to use.  Default is just
$ Poisson's/Continuity/Boltzman
$ - Can specify additional models or the temperature for the
$ simulation

MODELS ANALYTIC PRPMOB FLDMOB=2

$ Initial Solution
$ Symbolic factorization, solve, and save the solution

SYMB NEWTON CARRIERS=1 HOLE
```

```
METHOD ITLIMIT=1000 STACK=10
SOLVE V(Drain)=-1.5 V(Gate)=-3 OUT.FILE=MDGAAS1S

$ Impurity profile plots

PLOT.1D DOPING X.START=.25 X.END=.25 Y.START=0 Y.END=2
+ SYMBOL=2 COLOR=11 TITLE="pmos GaAs - Source Impurity Profile"
+ OUT.FILE="Source_Impurity_Profile"

PLOT.1D DOPING X.START=2 X.END=2 Y.START=0 Y.END=2
+ SYMBOL=2 COLOR=11 TITLE="pmos GaAs - Gate Impurity Profile"
+ OUT.FILE="Gate_Impurity_Profile"

PLOT.1D DOPING X.START=3.75 X.END=3.75 Y.START=0 Y.END=2
+ SYMBOL=2 COLOR=11 TITLE="pmos GaAs - Drain Impurity Profile"
+ OUT.FILE="Drain_Impurity_Profile"

PLOT.1D DOPING X.START=0 X.END=4 Y.START=0.01 Y.END=0.01
+ SYMBOL=2 COLOR=11 TITLE="pmos GaAs - Inpurity along channel"
+ OUT.FILE="Channel_Impurity_Profile"

$ and again using Y.LOG

PLOT.1D DOPING X.START=.25 X.END=.25 Y.START=0 Y.END=2
+ SYMBOL=2 COLOR=11 Y.LOG
+ TITLE="pmos GaAs - Source Impurity Profile"
+ OUT.FILE="Source_Impurity_Profile_LOG"

PLOT.1D DOPING X.START=2 X.END=2 Y.START=0 Y.END=2
+ SYMBOL=2 COLOR=11 Y.LOG
+ TITLE="pmos GaAs - Gate Impurity Profile"
+ OUT.FILE="Gate_Impurity_Profile_LOG"

PLOT.1D DOPING X.START=3.75 X.END=3.75 Y.START=0 Y.END=2
+ SYMBOL=2 COLOR=11 Y.LOG
```

```
+ TITLE="pmos GaAs - Drain Impurity Profile"
+ OUT.FILE="Drain_Impurity_Profile_LOG"

PLOT.1D DOPING X.START=0 X.END=4 Y.START=0.01 Y.END=0.01
+ SYMBOL=2 COLOR=11 Y.LOG
+ TITLE="pmos GaAs - Inpurity along channel"
+ OUT.FILE="Channel_Impurity_Profile_LOG"

$ Impurity contour plot

PLOT.2D BOUND TITLE="pmos GaAs - Impurity Contours" FILL SCALE

CONTOUR DOPING LOG MIN=16 MAX=20 DEL=.5 COLOR=2
CONTOUR DOPING LOG MIN=-16 MAX=-15 DEL=.5 COLOR=1 LINE=2

$ Plot to show contact resistance

PLOT.2D BOUND LUMPED TITLE="pmos GaAs - Lumped Resistance"

VECTOR J.HOLE

$ Save the mesh

SAVE MESH OUT.FILE=MDGAAS1MS
```

Appendix C
Si BSIM3 Model Card

Austria Micro Systems 0.6 μm silicon process.

```
//-----------------------------------
// SPECTRE DIRECT
// MOS transistor library file
//-----------------------------------
//library cmos
//section cmostm
//
// ---------------------------------
// Owner:  Austria Mikro Systeme
// HIT-Kit:  Digital
// *****************SIMULATION PARAMETERS *************
// ---------------------------------
// format :  Spectre (Spectre Direct)
// model :  MOS BSIM3v3
// process :  CUBEQWAVP
// revision :  B;
// extracted :  CUE 41667; 1998-08; ese(487)
// doc# :  9933011 REV_B
// ---------------------------------
// TYPICAL MEAN CONDITION
// ---------------------------------
```

```
//
inline subckt modn ( d g s b )
parameters w=1.0e-6 l=1.0e-6 nrd=0.0 nrs=0.0 ad=0.0
as=0.0 pd=0.0 ps=0.0
//
modn ( d g s b ) mosinsub w=w l=l nrd=nrd nrs=nrs
ad=ad as=as pd=pd ps=ps
model mosinsub bsim3v3 version=3.1 type=n capmod=2.000e+00 \
mobmod=1.000e+00 nqsmod=0.000e+00 noimod=1.000e+00 \
k1=1.057e+00 \
k2=-1.23e-01 k3=6.535e+00 k3b=-2.02e+00 \
nch=9.114e+16 vth0=8.481e-01 \
voff=-1.16e-01 dvt0=3.561e+00 dvt1=8.652e-01 \
dvt2=-2.50e-01 keta=-4.48e-02 \
pscbe1=3.616e+08 pscbe2=1.020e-05 \
dvt0w=-2.98e+00 dvt1w=1.306e+06 dvt2w=-9.24e-03 \
ua=1.000e-12 ub=1.709e-18 uc=-3.60e-11 \
u0=4.269e+02 \
dsub=5.000e-01 eta0=1.008e-02 etab=-1.72e-02 \
nfactor=6.529e-01 \
em=4.100e+07 pclm=9.549e-01 \
drout=3.510e-01 \
a0=9.550e-01 a1=0.000e+00 a2=1.000e+00 \
pvag=0.000e+00 vsat=8.665e+04 ags=1.785e-01 b0=2.652e-07 \
b1=0.000e+00 \
delta=1.000e-02 pdiblcb=2.306e-01 \
pdiblc1=2.750e-02 \
pdiblc2=1.069e-03 \
w0=3.151e-08 \
dlc=1.449e-07 \
dwc=-8.94e-09 dwb=0.000e+00 dwg=0.000e+00 \
ll=0.000e+00 lw=0.000e+00 lwl=0.000e+00 \
lln=1.000e+00 lwn=1.000e+00 wl=0.000e+00 \
```

```
ww=0.000e+00 wwl=0.000e+00 wln=1.000e+00 \
wwn=1.000e+00 \
at=3.300e+04 ute=-1.90e+00 \
kt1=-4.20e-01 kt2=2.200e-02 kt1l=0.000e+00 \
ua1=0.000e+00 ub1=0.000e+00 uc1=0.000e+00 \
prt=0.000e+00 \
cgdo=3.400e-10 cgso=3.400e-10 cgbo=1.300e-10 \
cgdl=0.000e+00 cgsl=0.000e+00 ckappa=6.000e-01 \
cf=0.000e+00 elm=5.000e+00 \
xpart=1.000e+00 clc=1.000e-15 cle=6.000e-01 \
rdsw=1.687e+03 \
cdsc=0.000e+00 cdscb=0.000e+00 cdscd=0.000e+00 \
prwb=0.000e+00 prwg=0.000e+00 cit=2.234e-04 \
tox=1.270e-08 \
ngate=0.000e+00 \
nlx=1.000e-10 \
xl=0.000e+00 xw=0.000e+00 \
af=1.343e+00 kf=6.896e-27 ef=1.000e+00 \
noia=1.000e+20 noib=5.000e+04 noic=-1.40e-12 \
rd=0.000e+00 rs=0.000e+00 rsh=3.000e+01 \
minr=1.000e-03 \
rdc=0.000e+00 rsc=0.000e+00 lint=1.449e-07 \
wint=-8.94e-09 ldif=0.000e+00 hdif=8.000e-07 \
xj=3.000e-07 js=2.000e-05 \
n=1.000e+00 \
dskip=no tlev=0 tlevc=0 \
cj=3.800e-04 cjsw=4.300e-10 \
fc=0.000e+00 fcsw=0.000e+00 \
mj=4.400e-01 mjsw=2.500e-01 \
pb=8.400e-01 pbsw=9.400e-01
ends modn
// ---------------------------------
// Owner:  Austria Mikro Systeme
```

```
// HIT-Kit:  Digital
// ****************** SIMULATION PARAMETERS ***********
// ---------------------------------
// format :  Spectre (Spectre Direct)
// model :  MOS BSIM3v3
// process :  CUBEQWAVP
// revision :  B;
// extracted :  CUE 41667; 1998-08; ese(487)
// doc# :  9933011 REV_B
// ---------------------------------
// TYPICAL MEAN CONDITION
// ---------------------------------
//
inline subckt modp ( d g s b )
parameters w=1.0e-6 l=1.0e-6 nrd=0.0 nrs=0.0 ad=0.0
as=0.0 pd=0.0 ps=0.0
//
modp ( d g s b ) mosinsub w=w l=l nrd=nrd nrs=nrs ad=ad
as=as pd=pd ps=ps
model mosinsub bsim3v3 version=3.1 type=p capmod=2.000e+00 \
mobmod=1.000e+00 nqsmod=0.000e+00 noimod=1.000e+00 \
k1=5.626e-01 \
k2=-1.66e-02 k3=1.485e+01 k3b=-1.40e+00 \
nch=5.948e+16 vth0=-7.85e-01 \
voff=-1.12e-01 dvt0=2.066e+00 dvt1=5.015e-01 \
dvt2=-3.99e-02 keta=-7.67e-03 \
pscbe1=5.000e+08 pscbe2=1.000e-10 \
dvt0w=0.000e+00 dvt1w=0.000e+00 dvt2w=0.000e+00 \
ua=6.770e-11 ub=1.040e-18 uc=-1.16e-10 \
u0=1.115e+02 \
dsub=4.379e-01 eta0=4.843e-02 etab=-3.50e-05 \
nfactor=2.220e-01 \
em=4.100e+07 pclm=1.459e+00 \
```

```
drout=7.861e-02 \
a0=7.522e-01 a1=0.000e+00 a2=1.000e+00 \
pvag=0.000e+00 vsat=9.496e+04 ags=1.746e-01 b0=3.421e-07\
b1=0.000e+00 \
delta=1.000e-02 pdiblcb=-3.18e-01 \
pdiblc1=5.872e-03 \
pdiblc2=3.394e-04 \
w0=7.289e-07 \
dlc=9.927e-08 \
dwc=3.878e-08 dwb=0.000e+00 dwg=0.000e+00 \
ll=0.000e+00 lw=0.000e+00 lwl=0.000e+00 \
lln=1.000e+00 lwn=1.000e+00 wl=0.000e+00 \
ww=0.000e+00 wwl=0.000e+00 wln=1.000e+00 \
wwn=1.000e+00 \
at=3.300e+04 ute=-1.40e+00 \
kt1=-5.70e-01 kt2=2.200e-02 kt1l=0.000e+00 \
ua1=0.000e+00 ub1=0.000e+00 uc1=0.000e+00 \
prt=0.000e+00 \
cgdo=3.400e-10 cgso=3.400e-10 cgbo=1.300e-10 \
cgdl=0.000e+00 cgsl=0.000e+00 ckappa=6.000e-01 \
cf=0.000e+00 elm=5.000e+00 \
xpart=1.000e+00 clc=1.000e-15 cle=6.000e-01 \
rdsw=3.796e+03 \
cdsc=0.000e+00 cdscb=0.000e+00 cdscd=2.171e-04 \
prwb=0.000e+00 prwg=0.000e+00 cit=3.231e-04 \
tox=1.270e-08 \
ngate=0.000e+00 \
nlx=2.784e-07 \
xl=0.000e+00 xw=0.000e+00 \
af=1.368e+00 kf=7.623e-29 ef=1.000e+00 \
noia=1.000e+20 noib=5.000e+04 noic=-1.40e-12 \
rd=0.000e+00 rs=0.000e+00 rsh=6.000e+01 \
minr=1.000e-03 \
```

```
rdc=0.000e+00 rsc=0.000e+00 lint=9.927e-08 \
wint=3.878e-08 ldif=0.000e+00 hdif=8.000e-07 \
xj=3.000e-07 js=2.000e-05 \
n=1.000e+00 \
dskip=no tlev=0 tlevc=0 \
cj=6.000e-04 cjsw=3.300e-10 \
fc=0.000e+00 fcsw=0.000e+00 \
mj=4.400e-01 mjsw=2.400e-01 \
pb=8.400e-01 pbsw=9.400e-01
ends modp
// -----------------------------------------------
```

Appendix D
Medici Device Code for GaAs NMOS

```
$ A simulation of an nmos device based on the Motorola
$ pmos GaAs device (26th) 5 May 2005
$ Sonia Paluchowski EngD Research Engineer

$ Specify a rectangular mesh*******************************

$ All distances in microns (WIDTH, DEPTH, L, H1, Y.MIN)

MESH SMOOTH=1
X.MESH WIDTH=4 H1=0.1

$ Mesh for the oxide
Y.MESH N=1 L=-0.009
Y.MESH N=10 L=0

$ Mesh varying with depth below oxide
Y.MESH DEPTH=0.002 H1=0.0001
Y.MESH DEPTH=0.031 H1=0.0005
Y.MESH DEPTH=0.003 H1=0.0001
Y.MESH DEPTH=0.004 H1=0.0005
Y.MESH DEPTH=0.050 H1=0.001
Y.MESH DEPTH=0.510 H1=0.01
Y.MESH DEPTH=0.400 H1=0.1
Y.MESH DEPTH=1 H1=0.5
```

```
$ Eliminate some unecessary mesh points
ELIMIN COLUMNS Y.MIN=1

$*********************************************************

$ Specify oxide, GaAs, AlGaAs and InGaAs regions**********
$ All distances in microns (Y.MIN, Y.MAX)

$ Structure as in paper
$ If 2ML = 0.5nm
REGION NAME=GA2O3 INSULATO Y.MAX=0
REGION NAME=GAASML GAAS Y.MIN=0 Y.MAX=0.0005
REGION NAME=ALGAAS ALGAAS Y.MIN=0.0005 Y.MAX=0.0155
+ X.MOLE=0.75
REGION NAME=INGAAS INGAAS Y.MIN=0.0155 Y.MAX=0.0305
+ X.MOLE=0.2
REGION NAME=GAAS GAAS Y.MIN=0.0305

$*********************************************************

$ Electrode definition************************************
$ All distances in microns (X.MIN, X.MAX)

$ Gate and substrate as paper
ELECTR NAME=Gate X.MIN=1.7 X.MAX=2.3 TOP
ELECTR NAME=Substrate BOTTOM

$ Source and drain width not given so sensible value chosen
ELECTR NAME=Source X.MAX=0.5 Y.MAX=0
ELECTR NAME=Drain X.MIN=3.5 Y.MAX=0

$*********************************************************

$ Specify the doping throughout the device***************
```

```
$ Doping quantities in cm-3 (N.PEAK)
$ All distances in microns (X.MIN, WIDTH, Y.MIN, Y.CHAR, Y.JUNC)

$ Specify substrate impurity-must be greater than GaAs ni=2.25e6
PROFILE P-TYPE N.PEAK=8E16 UNIFORM OUT.FILE=MDGAAS1DS

$ Delta Doping given in paper as 3.3e11 cm-2
$ => 3.3e11 cm-2 * 1e7 (1/1nm) cm-1 = 3.3e18 cm-3
$ If 2ML = 0.5nm
PROFILE P-TYPE UNIFORM Y.MIN=0.0335 DEPTH=0.001 N.PEAK=3.3e18

$ Specify Source and Drain Doping
$ 5e19 is the limit for S/D doping in GaAs
PROFILE N-TYPE N.PEAK=2.125E19 X.MIN=0.0 WIDTH=1.6
+ X.CHAR=0.01 Y.MIN=0 DEPTH=0.2 Y.CHAR=0.01
PROFILE N-TYPE N.PEAK=2.125E19 X.MIN=2.4 WIDTH=1.6
+ X.CHAR=0.01 Y.MIN=0 DEPTH=0.2 Y.CHAR=0.01

$************************************************************

$ Interface Trap Density
$ Trapped charge density for the electron acceptors in cm-2/eV
$ (N.ACCEPT)
$ INTERFACE REGION=(GA2O3,GAASML) N.ACCEPT=3E11

$ Plot the mesh
PLOT.2D GRID TITLE="nmos GaAs - Grid" FILL SCALE

$************************************************************

$ Defining Ga2O3 Material Properties*************************
$ Energy bandgap at 300K in eV (EG300)
$ Density in Kg/cm3 (DENSITY)

MATERIAL REGION=GA2O3 PERMITTI=10 EG300=4.9 DENSITY=0.006
```

```
$************************************************************

$Define permittivities*****************************************

MATERIAL REGION=ALGAAS PERMITTI=10.7
MATERIAL REGION=INGAAS PERMITTI=13.15

$************************************************************

$ Specify contact parameters***********************************
$ Workfunction of materials in V (WORKFUNC)
$ Resistance in Ohm-um (RESISTAN)

CONTACT NAME=Gate WORKFUNC=4.68

$ From paper - Contact resistance(1050)
$ + sheet resistance(1480.8) = 2530.8

CONTACT NAME=Source RESISTAN=2530.8
CONTACT NAME=Drain RESISTAN=2530.8

$************************************************************

$ Specify physical models to use.  Default is just
$ Poisson's/Continuity/Boltzman
$ - Can specify additional models or the temperature for the
$ simulation

MODELS ANALYTIC PRPMOB FLDMOB=2

$ Initial Solution
$ Symbolic factorization, solve, and save the solution

SYMB NEWTON CARRIERS=1 ELEC
```

```
METHOD ITLIMIT=1000 STACK=10
SOLVE V(Drain)=1.5 V(Gate)=3 OUT.FILE=MDGAAS1S

$ Impurity profile plots

PLOT.1D DOPING X.START=.25 X.END=.25 Y.START=0 Y.END=2
+ SYMBOL=2 COLOR=11 TITLE="nmos GaAs - Source Impurity Profile"

PLOT.1D DOPING X.START=2 X.END=2 Y.START=0 Y.END=2
+ SYMBOL=2 COLOR=11 TITLE="nmos GaAs - Gate Impurity Profile"

PLOT.1D DOPING X.START=3.75 X.END=3.75 Y.START=0 Y.END=2 Y.LOG
+ SYMBOL=2 COLOR=11 TITLE="nmos GaAs - Drain Impurity Profile"

PLOT.1D DOPING X.START=0 X.END=4 Y.START=0.01 Y.END=0.01 Y.LOG
+ SYMBOL=2 COLOR=11 TITLE="nmos GaAs - Inpurity along channel"

$ Impurity contour plot

PLOT.2D BOUND TITLE="nmos GaAs - Impurity Contours" FILL SCALE

CONTOUR DOPING LOG MIN=16 MAX=20 DEL=.5 COLOR=2
CONTOUR DOPING LOG MIN=-16 MAX=-15 DEL=.5 COLOR=1 LINE=2

$ Plot to show contact resistance

PLOT.2D BOUND LUMPED TITLE="nmos GaAs - Lumped Resistance"

VECTOR J.ELEC

$ Save the mesh

SAVE MESH OUT.FILE=MDGAAS1MS
```

Appendix E
BSIM3v3.2 Default Parameter Values

BSIM3v3.2 Process Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
t_{ox}	tox	Gate Oxide Thickness	1.5×10^{-8}	m
Toxm	toxm	Tox at which parameters are extracted	Tox	m
X_j	xj	Junction Depth	1.5×10^{-7}	m
γ_1	gamma1	Body-effect coefficient near the surface	calculated	$V^{1/2}$
γ_2	gamma2	Body-effect coefficient in the bulk	calculated	$V^{1/2}$
N_{ch}	nch	Channel doping concentration	1.7×10^{17}	$1/cm^3$
N_s	nsub	Substrate doping concentration	6×10^{16}	$1/cm^3$
V_{bx}	vbx	V_{bs} at which the depletion region width equals X_t	calculated	V

continued on next page

		continued from previous page		
Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
X_t	xt	Doping depth	1.55×10^{-7}	m

BSIM3v3.2 DC Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
V_{th}	vth0	Threshold voltage @ $V_{bs} = 0$ for large L	0.7 (NMOS) -0.7 (PMOS)	m m
V_{fb}	vfb	Flat-band voltage	calculated	V
K_1	k1	First order body coefficient	0.5	$V^{1/2}$
K_2	k2	Second order body coefficient	0.0	none
K3	k3	Narrow width coefficient	80.0	none
K3b	k3b	Body effect coefficient of k3	0.0	1/V
W0	w0	Narrow width parameter	2.5×10^{-6}	m
Nlx	nlx	Lateral non-uniform doping parameter	1.74×10^{-7}	m
V_{bm}	vbm	Maximum applied body bias in V_{th} calculation	-3.0	V
Dvt0	dvt0	First coefficient of short channel effect on V_{th}	2.2	none
Dvt1	dvt1	Second coefficient of short channel effect on V_{th}	0.53	none
Dvt2	dvt2	Body-bias coefficient of short channel effect on V_{th}	-0.032	1/V
		continued on next page		

continued from previous page

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Dvt0w	dvt0w	First coefficient of narrow width effect on Vth for small channel length	0	1/m
Dvt1w	dvt1w	Second coefficient of narrow width effect on Vth for small channel length	5.3×10^6	1/m
Dvt2w	dvt2w	Body-bias coefficient of narrow width effect for small channel length	-0.032	1/V
μ_0	u0	Mobility at Temp = T_{nom}	670.0 (NMOS) 250.0 (PMOS)	cm^2/Vs cm^2/Vs
μ_a	ua	First order mobility degradation coefficient	2.25×10^{-9}	m/V
μ_b	ub	Second order mobility degradation coefficient	5.87×10^{-19}	$(m/V)^2$
μ_c	Uc	Body-effect coefficient of mobility degredation coefficient	mobMod = 1, 2: -4.65×10^{-11} mobMod = 3: -0.046	 m/V^2 1/V
V_{sat}	vsat	Saturation velocity at Temp = T_{nom}	8×10^4	m/s
a_0	a0	Bulk charge effect coeffient for channel length	1.0	none
Ags	ags	Gate bias coefficient of A_{bulk}	0.0	1/V
B0	b0	Bulk charge effect coefficient for channel width	0.0	m
B1	b1	Bulk charge effect width offset	0.0	m

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Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Keta	keta	Body-bias coefficient of bulk charge effect	-0.047	1/V
A1	a1	First non-saturation effect parameter	0.0	1/V
A2	a2	Second non-saturation factor	1.0	none
R_{dsw}	rdsw	Parasitic resistance per unit width	0.0	$\Omega - \mu m^{W_r}$
Prwb	prwb	Body effect coefficient of R_{dsw}	0	$V^{-1/2}$
Prwg	prwg	Gate bias effect coefficient of R_{dsw}	0	1/V
Wr	wr	Width offset from Weff for Rds calculation	1.0	none
Wint	wint	Width offset fitting parameter from I-V without bias	0.0	m
L_{int}	lint	Length offset fitting parameter from I-V without bias	0.0	m
dWg	dwg	Coefficient of Weff's gate dependence	0.0	m/V
dWb	dwb	Coefficient of Weff's substrate body bias dependence	0.0	$m/V^{1/2}$
Voff	voff	Offset voltage in the subthreshold region at large W and L	-0.08	V
N_{factor}	nfactor	Subthreshold swing factor	1.0	none
η_0	eta0	DIBL coefficient in subthreshold region	0.08	none

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Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
η_b	etab	Body bias coefficient for the subthreshold DIBL effect	-0.07	1/V
D_{sub}	dsub	DIBL coefficient exponent in substreshold region	drout	none
Cit	cit	Interface trap capacitance	0.0	F/m^2
C_{dsc}	cdsc	Drain/source to channel coupling capacitance	2.4×10^{-4}	F/m^2
Cdscb	cdscb	Body bias sensitivity of C_{dsc}	0.0	F/Vm^2
Cdscd	cdscd	Drain bias sensitivity of C_{dsc}	0.0	F/Vm^2
P_{clm}	pclm	Channel length modulation parameter	1.3	none
Pdiblc1	pdiblc1	First output resistance DIBL effect correction parameter	0.39	none
Pdiblc2	pdiblc2	Second output resistance DIBL effect correction parameter	0.0086	none
Pdiblcb	pdiblcb	Body effect coefficient of DIBL correction parameters	0	1/V
D_{rout}	drout	L dependence coefficient of the DIBL correction parameter in Rout	0.56	none
Pscbe1	pseb1	First substrate current body effect parameter	4.24×10^8	V/m
Pscbe2	pseb2	Second substrate current body effect parameter	1.05×10^{-5}	m/V
Pvag	pvag	Gate dependence of early voltage	0.0	none

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Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
δ	delta	Effective V_{ds} parameter	0.01	V
Ngate	ngate	Poly gate doping concentration	0	cm^{-3}
$\alpha 0$	alpha0	The first parameter of impact ionization current	0	m/V
$\alpha 1$	alpha1	Isub parameter for length scaling	0.0	1/V
$\beta 0$	beta0	The second parameter of impact ionization current	30	V
R_{sh}	rsh	Source drain sheet resistance in ohm per square	0.0	Ω/sq
Jsw	jsw	Side wall saturation density	0.0	A/m
Js	js	Source drain junction saturation current per unit area	1×10^{-4}	A/m^2
ijth	ijth	Diode limiting current	0.1	A

BSIM3v3.2 C-V Model Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
X_{part}	xpart	Charge partitioning flag	0.0	none
C_{gs0}	cgs0	Non LDD region source-gate overlap capacitance per channel length	calculated	F/m
		continued on next page		

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Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
C_{gd0}	cgd0	Non LDD region drain-gate overlap capacitance per channel length	calculated	F/m
CGB0	cgb0	Gate bulk overlap capacitance per unit channel length	0.0	F/m
C_j	cj	Bottom junction capacitance per unit area at zero bias	5.0×10^{-4}	F/m^2
Mj	mj	Bottom junction capacitance grating coefficient	0.5	none
Mjsw	mjsw	Source/drain side wall junction capacitance grading coefficient	0.33	none
Cjsw	cjsw	Source/drain side wall junction capacitance per unit area	5×10^{-10}	F/m
Cjswg	cjswg	Source/drain side wall junction capacitance grading coefficient	Cjsw	F/m
Mjswg	mjswg	Source/drain gate side wall junciton capacitance grading coefficient	Mjsw	none
Pbsw	pbsw	Source/drain side wall junction built-in potential	1.0	V
Pb	pb	Bottom built-in potential	1.0	V
Pbswg	pbswg	Source/drain gate side wall junction built-in potential	Pbsw	V
CGS1	cgs1	Light doped source-gate region overlap capacitance	0.0	F/m

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Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
CGD1	cgd1	Light doped drain-gate region overlap capacitance	0.0	F/m
C_κ	ckappa	Coefficient for lightly doped region overlap capacitance	0.6	F/m
C_f	cf	Fringing field capacitance	calculated	F/m
CLC	clc	Constant term for the short channel model	0.1×10^{-6}	m
CLE	cle	Exponential term for the short channel model	0.6	none
DLC	dlc	Length offset fitting parameter from C-V	lint	m
DWC	dwc	Width offset fitting parameter from C-V	wint	m
noff	noff	CV parameter in Vgsteff, CV for weak to strong inversion	1.0	none
voffcv	voffcv	CV parameter in Vgsteff, CV for week to strong inversion	0.0	V
acde	acde	Exponential coefficient for charge thickness in capMod=3 for accumulation and depletion regions	1.0	m/V
moin	moin	Coefficient for the gate-bias dependant surface potential	15.0	$V^{1.2}$

BSIM3v3.2 Model Control Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
None	level	The model selector	8	none
None	version	Model version selector	3.2	none
None	binUnit	Binning unit selector	1	none
None	paramChk	Parameter value check	False	none
mobMod	mobMod	Mobility model selector	1	none
capMod	capMod	Flag for capacitance models	3	none
nqsMod	nqsMod	Flag for NQS model	0	none
noiMod	noiMod	Flag for noise models	1	none

BSIM3v3.2 NQS Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Elm	elm	Elmore constant for the channel	5	none

BSIM3v3.2 dW and dL Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Wl	wl	Coefficient of length dependence for width offset	0.0	m^{Wln}
Wln	wln	Power of length dependence of width offset	1.0	none

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Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Ww	ww	Coefficient of width dependence for width offset	0.0	m^{Wwn}
Wwn	wwn	Power of width dependence of width offset	1.0	none
Wwl	wwl	Coefficient of length and width cross term for width offset	0.0	$m^{Wwn+Wln}$
Ll	ll	Coefficient of length dependence for length offset	0.0	m^{Lln}
Lln	lln	Power of lenght dependence for length offset	1.0	none
Lw	lw	Coefficient of width dependence for length offset	0.0	m^{Lwn}
Lwn	lwn	Power of width dependence for length offset	1.0	none
Lwl	lwl	Coefficient of length and width cross term for length offset	0.0	$m^{Lwn+Lln}$
Llc	Llc	Coefficient of length dependence for CV channel length offset	Ll	m^{Lln}
Lwc	Lwc	Coefficient of width dependence for CV channel length offset	Lw	m^{Lwn}
Lwlc	Lwlc	Coefficient of length and width dependence for CV channel lenght offset	Lwl	$m^{Lwn+Lln}$
Wlc	Wlc	Coefficient of length dependence for CV channel width offset	Wl	m^{Wln}

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Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Wwc	Wwc	Coefficient of width dependence for CV channel width offset	Ww	m^{Wwn}
Wwlc	Wwlc	Coefficient of length and width dependence for CV channel width offset	Wwl	$m^{Wln+Wwn}$

BSIM3v3.2 Temperature Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Tnom	tnom	Temperature at which parameters are extracted	27	° C
μte	ute	Mobility temperature exponent	-1.5	none
Kt1	kt1	Temperature coefficient for threshold voltage	-0.11	V
Kt1l	kt1l	Channel length dependence of the temperature coefficient for threshold voltage	0.0	Vm
Kt2	kt2	Body-bias coefficient of V_{th} temperature effect	0.022	none
Ua1	ua1	Temperature coefficient for Ua	4.31×10^{-9}	m/V
Ub1	ub1	Temperature coefficient for Ub	-7.61×10^{-18}	$(m/V)^2$

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Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Uc1	uc1	Temperature coefficient for Uc	mobMod = 1, 2: -5.6×10^{-11} mobMod = 3: -0.056	m/v^2 1/V
At	at	Temperature coefficient for saturation velocity	3.3×10^4	m/s
Prt	prt	Temperature coefficient for R_{dsw}	0.0	Ω-μm
nj	nj	Emission coefficient of junction	1.0	none
XTI	xti	Junction current temperature exponent coefficient	3.0	none
tpb	tpb	Temperature coefficient of Pb	0.0	W/K
tpbsw	tpbsw	Temperature coefficient of Pbsw	0.0	V/K
tpbswg	tpbswg	Temperature coefficient of Pbswg	0.0	V/K
tcj	tcj	Temperature coefficient of C_j	0.0	1/K
tcjsw	tcjsw	Temperature coefficient of Cjsw	0.0	1/K
tcjswg	tcjswg	Temperature coefficient of Cjswg	0.0	1/K

BSIM3v3.2 Flicker Noise Model Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Noia	noia	Noise parameter A	9.9×10^{18} (PMOS) 1×10^{20} (NMOS)	none none
Noib	noib	Noise parameter B	2.4×10^{3} (PMOS) 5×10^{4} (NMOS)	none none
Noic	noic	Noise parameter C	1.4×10^{-12} (PMOS) -1.4×10^{-12} (NMOS)	none none
Em	em	Saturation field	4.1×10^{7}	V/m
Af	af	Flicker noise exponent	1	none
Ef	ef	Flicker noise frequency exponent	1	none
Kf	kf	Flicker noise coefficient	0	none

BSIM3v3.2 Geometry Range Parameters

Symbol Used in Equations	Symbol Used in SPICE	Description	Default	Unit
Lmin	lmin	Minimum channel length	0.0	m
Lmax	lmax	Maximum channel length	1.0	m
Wmin	wmin	Mimimum channel width	0.0	m
Wmax	wmax	Maximum channel width	1.0	m
binUnit	binunit	Bin unit scale selector	1.0	none

Appendix F
GaAs BSIM3v3.2 Model Card

```
//---------------------------------------
// FILE HEADER
//---------------------------------------
//
// File Name :  gaas_model.scs
//
// Description :  Spectre Direct GaAs Model Library File
//
//---------------------------------------
// FILE CHANGE HISTORY
//---------------------------------------
//
// DATE BY DESCRIPTION
//---------------------------------------
// 20-Sept-2005 SHP Updated all PMOS and NMOS parameters.
//
//---------------------------------------
//
//---------------------------------------
// BEGIN THE LIBRARY
//---------------------------------------
//
library gaas_model
```

```
//
//--------------------------------------
// SECTION
//--------------------------------------
//
section gaas_tm
//
//--------------------------------------
// MODEL
//--------------------------------------
//
// n-channel MOSFET.
//
inline subckt modn ( d g s b )
parameters w=10e-6 l=0.6e-6 as=0 ad=0 ps=0 pd=0 nrs=0 nrd=0
//
modn ( d g s b ) mosinsub w=w l=l as=(2*w*l) ad=(2*w*l)
ps=(2*(2*(w+l))) pd=(2*(2*(w+l)))
model mosinsub bsim3v3 type=n \
level=49 \
version=3.2 \
binunit=1 \
paramchk=0 \
mobmod=1 \
capmod=3 \
nqsmod=0 \
noimod=2 \
vth0=0.93 \
k1=0.454 \
k2=0 \
k3=0 \
k3b=0 \
w0=2.5e-6 \
```

```
nlx=1.74e-7 \
vbm=-3 \
dvt0=2.2 \
dvt1=0.53 \
dvt2=-0.032 \
dvt0w=0 \
dvt1w=5.3e+6 \
dvt2w=-3.2e-2 \
u0=1500 \
ua=0.1e-8 \
ub=0 \
uc=0 \
vsat=1e+5 \
a0=0.199 \
ags=0 \
b0=0 \
b1=0 \
keta=-0.047 \
a1=0 \
a2=1 \
rdsw=1.05e+3 \
prwg=0 \
prwb=0 \
wr=1 \
wint=0 \
lint=0 \
dwg=0 \
dwb=0 \
voff=-0.08 \
nfactor=0.012 \
eta0=0 \
etab=0 \
dsub=0.0613 \
```

```
cit=0 \
cdsc=6.15e-3 \
cdscd=0 \
cdscb=0 \
pclm=1 \
pdiblc1=0.39 \
pdiblc2=0.0086 \
pdiblcb=0 \
drout=0.0613 \
pscbe1=4.24e+8 \
pscbe2=1e-5 \
pvag=0 \
delta=0.01 \
ngate=0 \
alpha0=0 \
alpha1=0 \
beta0=30 \
rsh=1234 \
jsw=0 \
js=1e-4 \
ijth=0.1 \
xpart=1 \
cgso=3.45e-10 \
cgdo=3.45e-10 \
cgbo=0 \
cj=7.7e-4 \
mj=0.5 \
mjsw=0.33 \
cjsw=5e-10 \
cjswg=5e-10 \
mjswg=0.33 \
pbsw=1 \
pb=1 \
```

```
pbswg=1 \
cgsl=0 \
cgdl=0 \
ckappa=0 \
cf=0 \
clc=0 \
cle=1 \
dlc=0 \
dwc=0 \
noff=1 \
voffcv=0 \
acde=9.14 \
moin=15 \
elm=5 \
wl=0 \
wln=1 \
ww=0 \
wwn=1 \
wwl=0 \
ll=0 \
lln=1 \
lw=0 \
lwn=1 \
lwl=0 \
llc=0 \
lwc=0 \
lwlc=0 \
wlc=0 \
wwc=0 \
wwlc=0 \
tnom=27 \
ute=-1.5 \
kt1=-0.11 \
```

```
kt1l=0 \
kt2=0.022 \
ua1=4.31e-9 \
ub1=-7.61e-18 \
uc1=-0.056 \
at=3.3e+4 \
prt=0 \
n=1 \
xti=3 \
tpb=0 \
tpbsw=0 \
tpbswg=0 \
tcj=0 \
tcjsw=0 \
tcjswg=0 \
noia=1e+20 \
noib=5e+4 \
noic=-1.4e-12 \
em=4.1e7 \
af=1 \
ef=1 \
kf=0 \
tox=9e-9 \
toxm=9e-9 \
xj=1.512e-7 \
gamma1=0.454 \
gamma2=0.454 \
nch=5.579e+20 \
nsub=5.579e+20 \
vbx=1.24 \
xt=19e-9 \
lmin=0 \
lmax=1 \
```

```
wmin=0 \
wmax=1
ends modn
//
//---------------------------------------
// MODEL
//---------------------------------------
//
// p-channel MOSFET.
//
inline subckt modp ( d g s b )
parameters w=10e-6 l=0.6e-6 as=0 ad=0 ps=0 pd=0 nrs=0 nrd=0
//
modp ( d g s b ) mosinsub w=w l=l as=(2*w*l) ad=(2*w*l)
ps=(2*(2*(w+l))) pd=(2*(2*(w+l)))
model mosinsub bsim3v3 type=p \
level=49 \
version=3.2 \
binunit=1 \
paramchk=0 \
mobmod=1 \
capmod=3 \
nqsmod=0 \
noimod=2 \
vth0=-0.93 \
k1=0.454 \
k2=0 \
k3=0 \
k3b=0 \
w0=2.5e-6 \
nlx=1.74e-7 \
vbm=-3 \
dvt0=2.2 \
```

```
dvt1=0.53 \
dvt2=-0.032 \
dvt0w=0 \
dvt1w=5.3e+6 \
dvt2w=-3.2e-2 \
u0=240 \
ua=0.53e-8 \
ub=0 \
uc=0 \
vsat=1e+5 \
a0=0.199 \
ags=0 \
b0=0 \
b1=0 \
keta=-0.047 \
a1=0 \
a2=1 \
rdsw=1.05e+3 \
prwg=0 \
prwb=0 \
wr=1 \
wint=0 \
lint=0 \
dwg=0 \
dwb=0 \
voff=-0.08 \
nfactor=0.012 \
eta0=0 \
etab=0 \
dsub=0.0613 \
cit=0 \
cdsc=6.15e-3 \
cdscd=0 \
```

```
cdscb=0 \
pclm=1 \
pdiblc1=0.39 \
pdiblc2=0.0086 \
pdiblcb=0 \
drout=0.0613 \
pscbe1=4.24e+8 \
pscbe2=1e-5 \
pvag=0 \
delta=0.01 \
ngate=0 \
alpha0=0 \
alpha1=0 \
beta0=30 \
rsh=1234 \
jsw=0 \
js=1e-4 \
ijth=0.1 \
xpart=1 \
cgso=3.45e-10 \
cgdo=3.45e-10 \
cgbo=0 \
cj=7.7e-4 \
mj=0.5 \
mjsw=0.33 \
cjsw=5e-10 \
cjswg=5e-10 \
mjswg=0.33 \
pbsw=1 \
pb=1 \
pbswg=1 \
cgsl=0 \
cgdl=0 \
```

```
ckappa=0 \
cf=0 \
clc=0 \
cle=1 \
dlc=0 \
dwc=0 \
noff=1 \
voffcv=0 \
acde=9.14 \
moin=15 \
elm=5 \
wl=0 \
wln=1 \
ww=0 \
wwn=1 \
wwl=0 \
ll=0 \
lln=1 \
lw=0 \
lwn=1 \
lwl=0 \
llc=0 \
lwc=0 \
lwlc=0 \
wlc=0 \
wwc=0 \
wwlc=0 \
tnom=27 \
ute=-1.5 \
kt1=-0.11 \
kt1l=0 \
kt2=0.022 \
ua1=4.31e-9 \
```

```
ub1=-7.61e-18 \
uc1=-0.056 \
at=3.3e+4 \
prt=0 \
n=1 \
xti=3 \
tpb=0 \
tpbsw=0 \
tpbswg=0 \
tcj=0 \
tcjsw=0 \
tcjswg=0 \
noia=9.9e+18 \
noib=2.4e+3 \
noic=1.4e-12 \
em=4.1e7 \
af=1 \
ef=1 \
kf=0 \
tox=9e-9 \
toxm=9e-9 \
xj=1.512e-7 \
gamma1=0.454 \
gamma2=0.454 \
nch=5.579e+20 \
nsub=5.579e+20 \
vbx=1.24 \
xt=19e-9 \
lmin=0 \
lmax=1 \
wmin=0 \
wmax=1 ends modp //
//-------------------------------------
```

```
// END THE SECTION
//-------------------------------------
//
endsection
//
//-----------------------------------------
// END THE LIBRARY
//-----------------------------------------
//
endlibrary
```

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